Design of Communication ICs

台大電子所　李致毅教授

Professor Jri Lee

National Taiwan University

關於這堂課...

- 三不
  不點名, 不小考, 不交作業
- 成績計算
  TBD
- 上課時間地點
  Monday 234, 博理112
- 助教
  吳克中/王懷德, 博理**R424**
- 參考書籍

"Design of Integrated Circuits for Optical communications"(30%)

"RF Microelectronics" (30%)

期刊論文/發明專利/吾所獨見而創獲者**(40%)**

關於這堂課…

- 授課內容

  Wireline: TIA, LA, MUX/DEMUX, Equalizer, CDR

  Wireless: LNA, PA, Mixer, Frequency Synthesizer

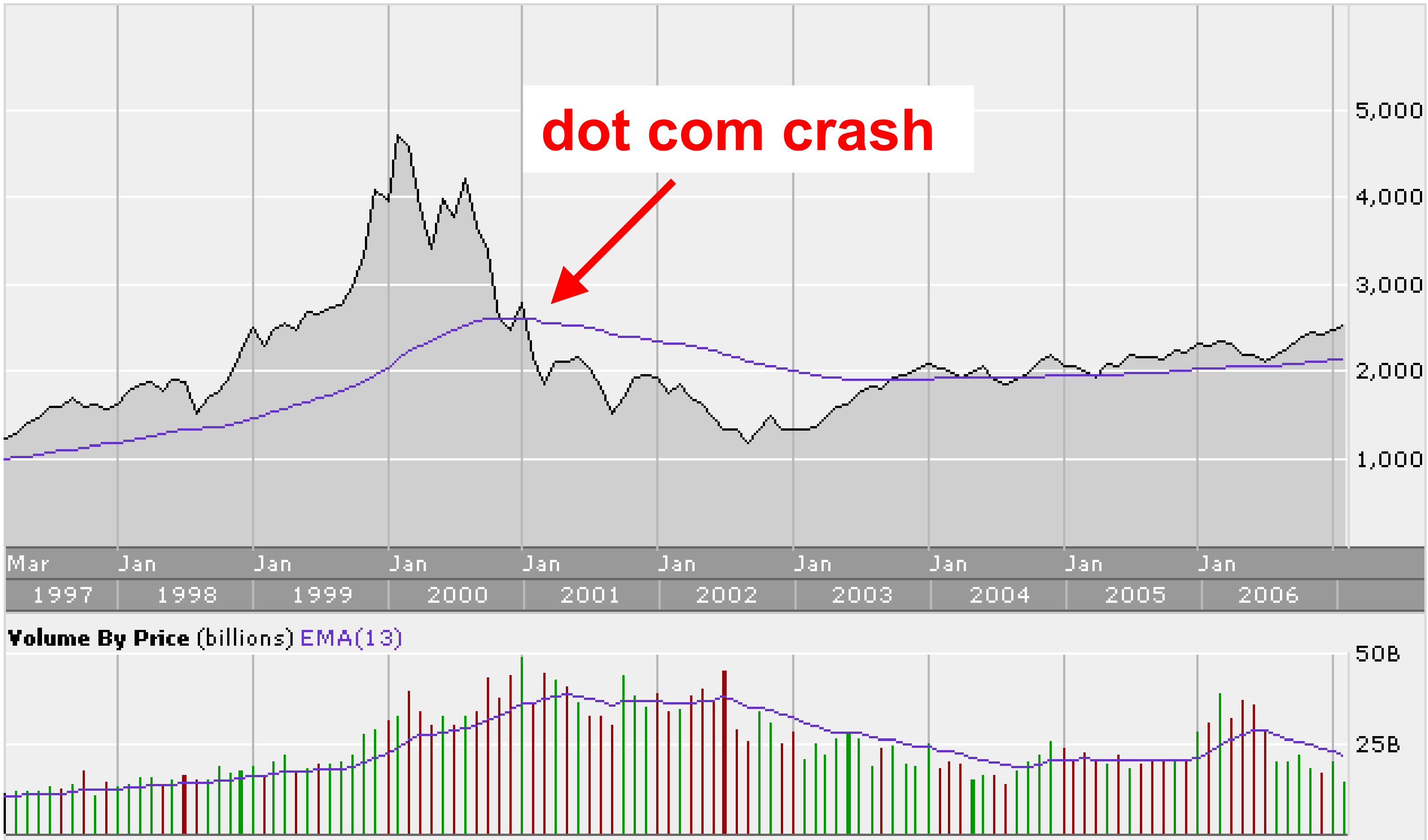
  General: Oscillator, Frequency Divider, PLL

- 授課方式

  投影片**+** 板書

  專題演講 **(3~4**次**)**

Nasdaq Index over the Past Decade



It is a Communication World

- Among the 33 sessions of ISSCC 2007, more than half of them are communication-related:

Wireline: 3~5	Analog: 1
Wireless/RF: 7-9	Technology Direction: 1
Baseband: 1	Data conversion: 2

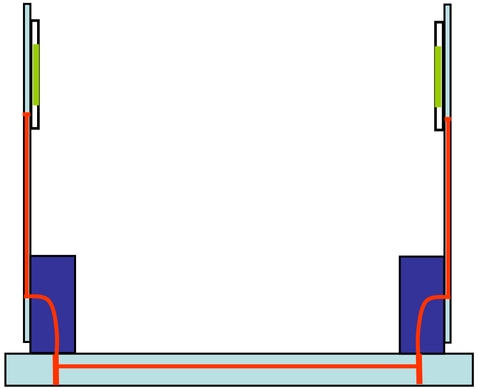
- One of the fields that updates itself most frequently.

  Example: Bluetooth, WLAN.
  Oscillators/PLLs speed up 10 times per decade.

- Market/capital/technology oriented.

Wireline Communication

- Optical
  SONET/OC
  PON
- Backplane
  Chip-to-Chip
  Board-to-Board
- Cable/Wire
  Ethernet
  Twisted Pair



- Exploring the (electronic) bandwidth limitation
  => use raw, un-modulated data (e.g., NRZ)
- In this course, we primarily focus on the (analog) front-end designs.

Why Optical Fibers?

- Modern optical communication fibers exhibit a bandwidth of 25 to 50 GHz and a loss of only 0.15 to 0.2 dB/km, presenting an overwhelming advantage over other media.

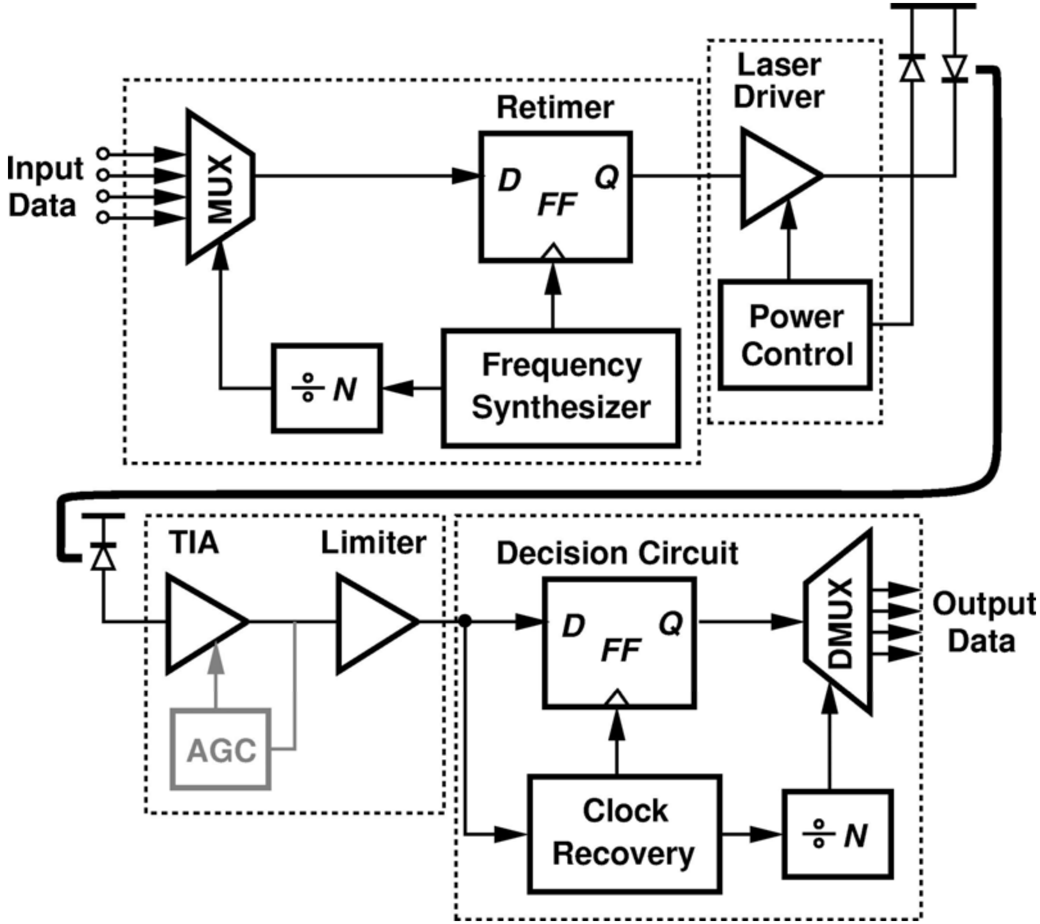
- Optical communications provide an ultimate solution for carrying large volumes of data across a long distance.

Comparison of Modern Communication Systems

	Data Rate	Loss (Range)
GSM	9.6 kb/s	500 m
WLAN(802.11a)	54 Mb/s	100 m
UWB	200 Mb/s	10 m
Twisted-Pair	12 Mb/s (ADSL)	200 dB/km
Coaxial	100 Mb/s	500 dB/km
Fiber (OC-192)	10 Gb/s	0.2 dB/km

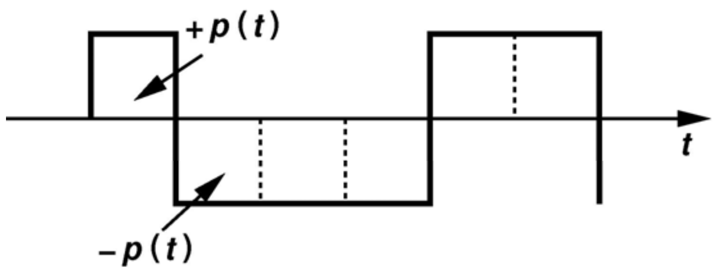
- Fiber provides ultimate bandwidth solution.

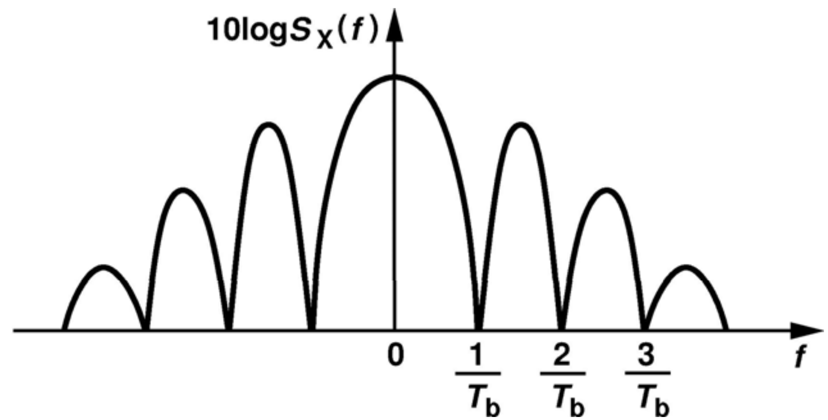
Typical Optical Communication Systems



- A transmitter, a receiver, and fiber channel are included.
- Individual blocks pose difficult challenges.

Basic Concepts of Random Binary Data

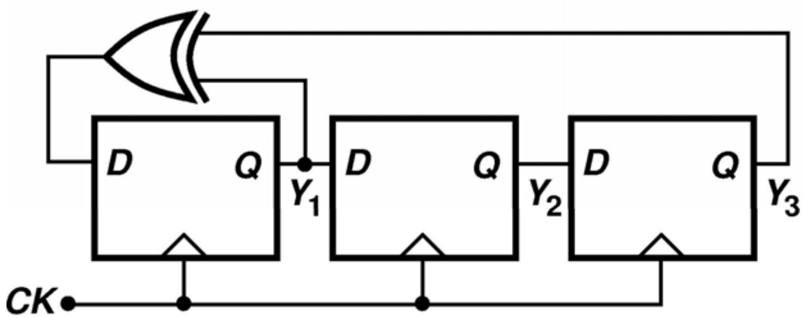




$$x(t) = \sum_k b_k p(t - kT_b) \quad \Longleftrightarrow \quad S_x(f) = T_b \left[\frac{\sin(\pi f T_b)}{\pi f T_b}\right]^2$$

- The spectrum exhibits no power at frequency of $1/T_b$ and its harmonics, suggesting difficulties on clock recovery.

Generation of Pseudo Random Binary Data

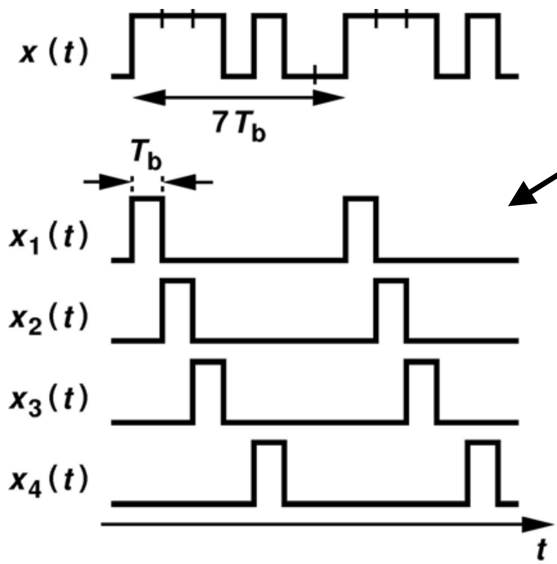


Y_1	Y_2	Y_3
1	0	0
1	1	0
1	1	1
0	1	1
1	0	1
0	1	0
0	0	1

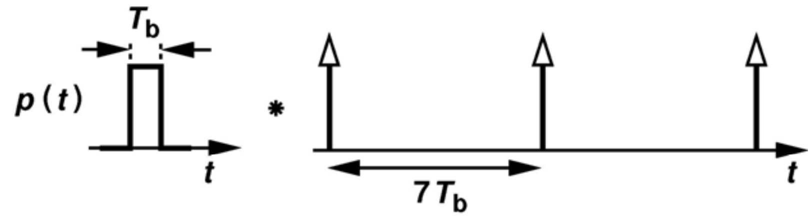
Length = $2^3 - 1$

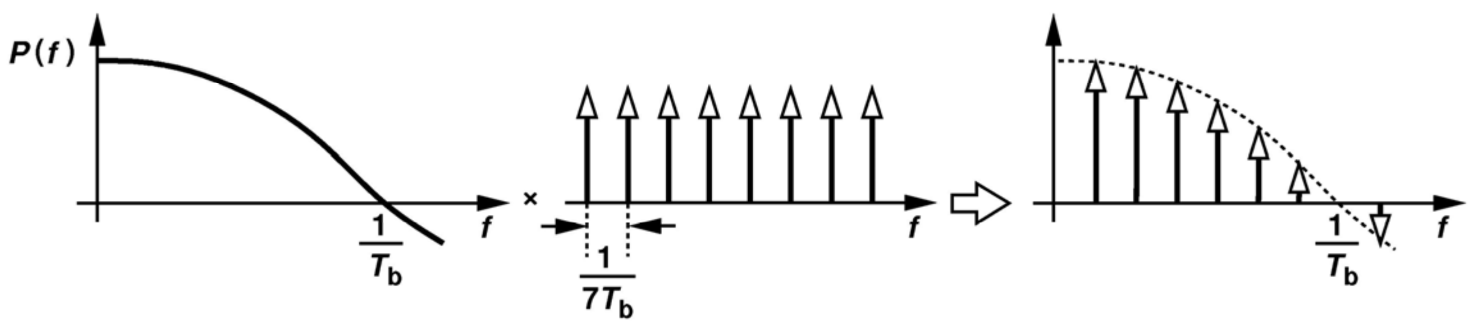
- **A sequence of length $2^m - 1$ contains at most m-bit runs.**
- **Longer sequence can be obtained by extending the number of shift registers.**
- **PRBS $2^{15} - 1$: $y^{15} \oplus y^{14} \oplus 1$,**
  PRBS $2^{23} - 1$: $y^{23} \oplus y^{18} \oplus 1$.

Spectrum of PRBS



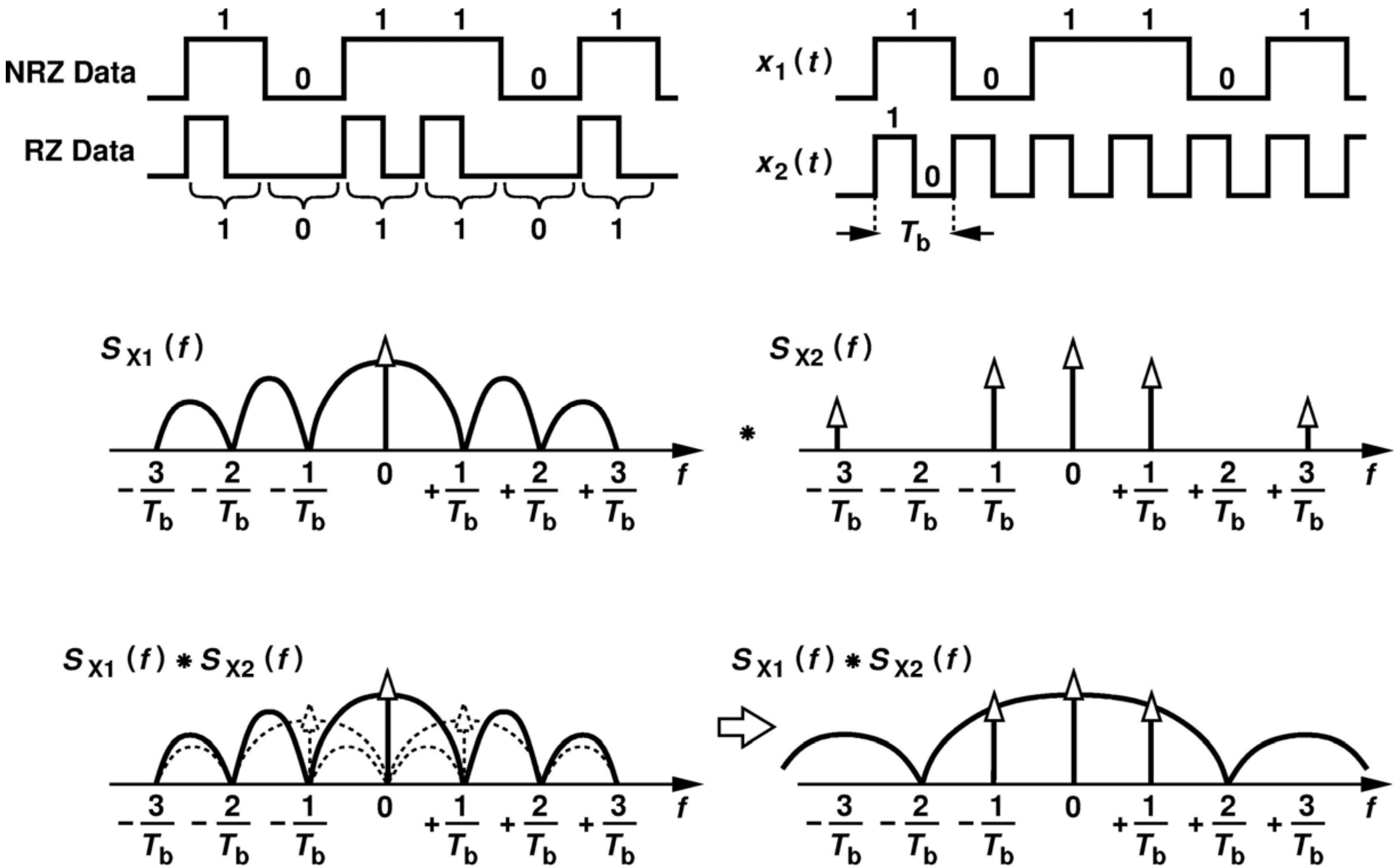
Pseudo Random Data Sequence
= Combination of Periodic Pulses





❒ The longer the random patterns, the closer the impulses.

Distinction between NRZ and RZ Data

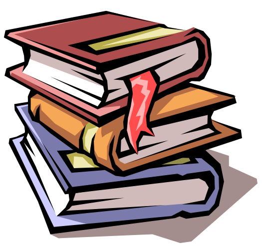


- RZ data occupies twice as much bandwidth.

Transimpedance Amplifiers

Professor Jri Lee

台大電子所　李致毅教授



Electrical Engineering Department

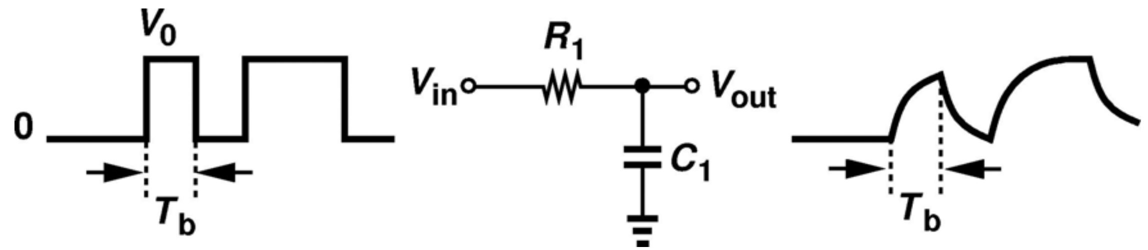
National Taiwan University

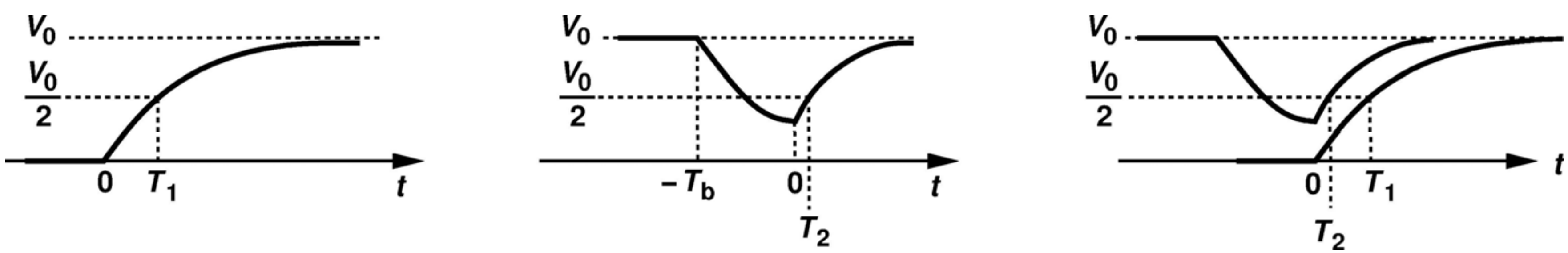
Outline

- General Considerations
- Open-Loop TIAs
- Feedback TIAs
- High Performance TIAs
- Case Study

Jitter Due to Bandwidth Limitation

- Insufficient bandwidth leads to deterministic jitter



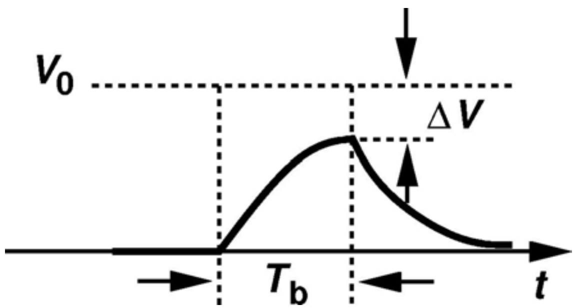


$$T_1 = \tau \ln 2$$

$$T_2 = \tau \ln[2(1 - \exp\frac{-T_b}{\tau})]$$

$$\frac{T_1 - T_2}{T_b} = \frac{-\tau}{T_b}\ln(1 - \exp\frac{-T_b}{\tau})$$

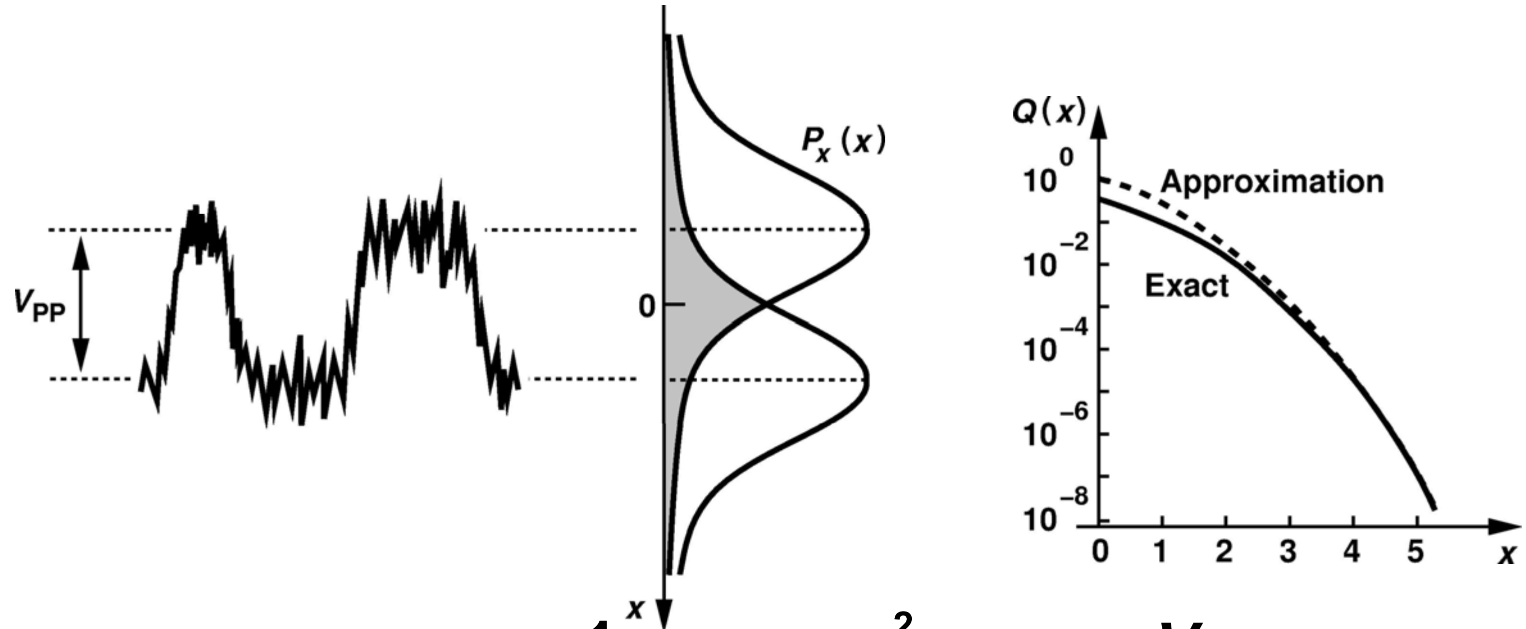
ISI Due to Bandwidth Limitation



$$\text{ISI} = \frac{\Delta V}{V_0} = \exp\frac{-T_b}{\tau}$$

- **Intersymbol Interference (ISI): defining the vertical eye closure.**
- **For a simple RC network with f_{-3dB} = 0.7 R_b, data jitter equals 0.28 % and ISI = 1.23 %.**
- **Practical TIAs contain multiple poles/zeros, making the analysis complex and requiring simulations.**

Noise Effect

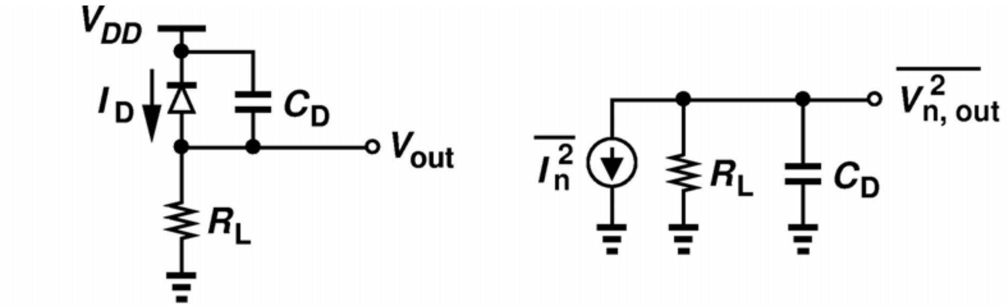


$$P_{c,tot} = \int_{V_0/\sigma_n}^{\infty} \frac{1}{\sqrt{2\pi}} \exp\frac{-x^2}{2} dx = Q\left(\frac{V_{PP}}{2\sigma_n}\right)$$

$$Q(x) = \int_{x}^{\infty} \frac{1}{\sqrt{2\pi}} \exp\frac{-u^2}{2} du \approx \frac{1}{x\sqrt{2\pi}} \exp\frac{-x^2}{2} \quad \text{for } x > 3$$

- For a BER of 10^{-12}, SNR needs to be around 14.
- Noise issue becomes more severe for low supply-voltage designs.

Single-Register TIAs



$$R_T(\text{Transimpedance Gain}) = R_L$$

$$\overline{I^2_{n,in}} = \frac{kT}{R_L^2 C_D}$$

$$\text{Data Rate} = \frac{1}{2\pi R_L C_D}$$

- Simplest way to convert current into voltage.
- Direct trade off between speed and noise ⇒ seeking circuits that provide low input resistance (high bandwidth) and high gain.

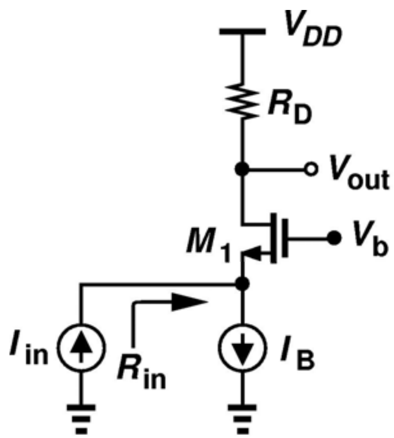
Typical TIA Specs for OC-192 (10 Gb/s)

Gain	> 1 kΩ
Bandwidth	> 9 GHz
Sensitivity	< -18 dBm
Maximum Input	> 3 dBm
Peaking	< 2 dB

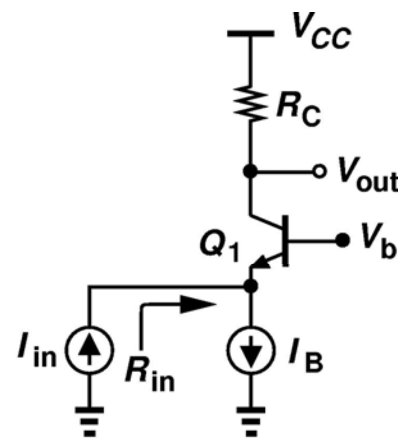
Challenges:

- High Gain
- Large Input Range
- Low Noise
- High Bandwidth
- Good PSRR
- Reasonable Power

Open-Loop TIAs



Common Gate



Common Base

$$R_T = R_D$$

$$R_{in} \approx \frac{1}{g_m + g_{mb}} + \frac{R_D}{(g_m + g_{mb})r_o}$$

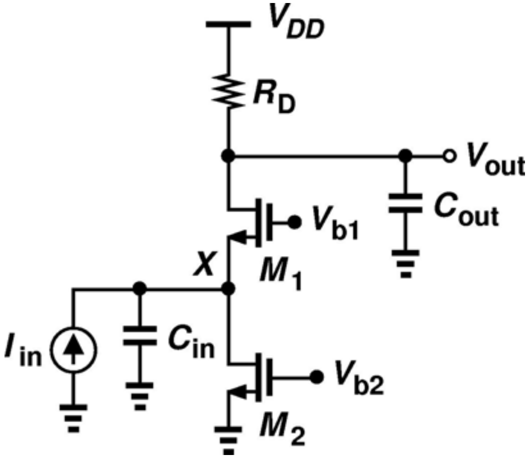
$$R_T = R_C$$

$$R_{in} \approx \frac{1}{g_m} + \frac{R_C}{g_m r_o}$$

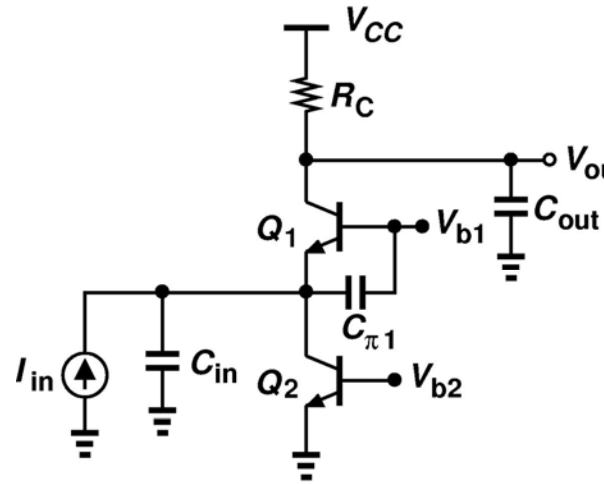
- **Satisfying (input) impedance matching.**
- **Comparable gain (consumes voltage headroom, too).**

High Frequency Response of Open-Loop TIAs

Common Gate



Common Base

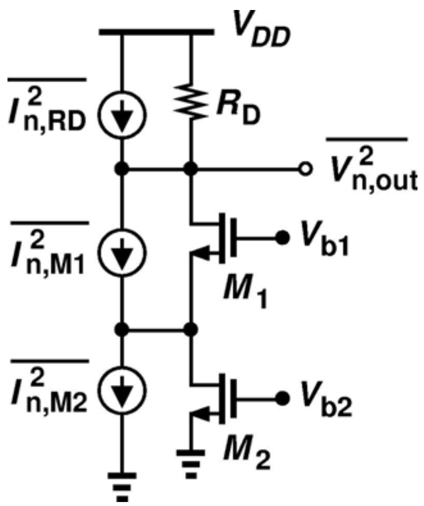


$$\frac{V_{out}}{I_{in}} = \frac{(g_{m1}+g_{mb1})R_D}{(g_{m1}+g_{mb1}+C_{in}s)(R_D C_{out}s+1)}$$

$$\frac{V_{out}}{I_{in}} = \frac{g_{m1}R_C}{(g_{m1}+C_{in}s)(R_D C_{out}s+1)}$$

- **Input pole dominates (C_{in} ~ 250 fF).**
- **Multiple tradeoffs make it difficult to achieve broad band and high gain simultaneously.**

Noise Performance of Common-Gate Stages



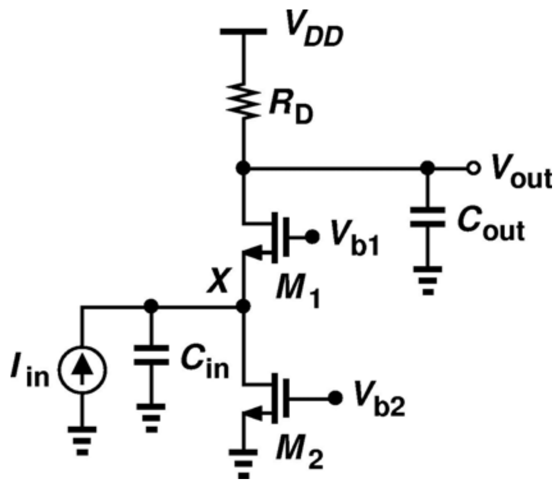
$$\overline{I^2_{n,in}} = 4kT(\gamma g_{m2} + \frac{1}{R_D})$$

$$= \overline{I^2_{n,M_2}} + \overline{I^2_{n,R_D}}$$

$$\frac{4kT}{\overline{\overline{I^2_{n,R_D}}}} + \frac{8kT\gamma}{\overline{\overline{I^2_{n,M_2}}}} < \frac{V_{DD}}{I_{D2}}$$

- Noise Currents of M_2 and R_D are referred to the input with unity gain and trade with each other.
- Noise can't be arbitrarily small $\Rightarrow$ performance limitation exists.
- For more information about noise, check: "Design of Analog CMOS Integrated Circuits", Chap 7.

High Frequency Noise Analysis of CG Stages



$$\overline{I^2_{n,in,tot}} = 4kT\gamma\left(\frac{1}{4}g_{m1}\omega_{p,out} + \frac{1}{2}g_{m2}\omega_{p,in}\right)$$

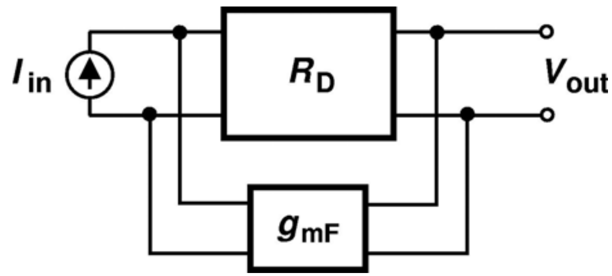
$$\omega_{p,in} = \frac{g_{m1} + g_{mb1}}{C_{in}}$$

$$\omega_{p,out} = \frac{1}{R_D C_{out}}$$

- ❒ Little flexibility can be achieved in CG/CB TIAs.
- ❒ CG/CB architecture bears intrinsic limitation in many aspects.

Feedback TIAs

- Consider a shunt-shunt feedback system:



$$R_T = \frac{R_D}{1 + R_D g_{mF}} \longrightarrow \text{Reasonable Gain}$$

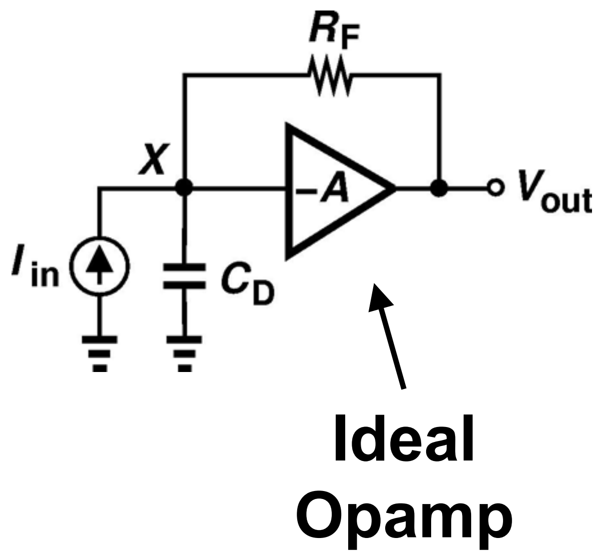
$$R_{in} = \frac{R_{in,open}}{1 + R_D g_{mF}}$$

$$R_{out} = \frac{R_{out,open}}{1 + R_D g_{mF}}$$

} Impedance Matching

- Many restrictions in CG/CB topology would be released.

First-Order Feedback TIAs

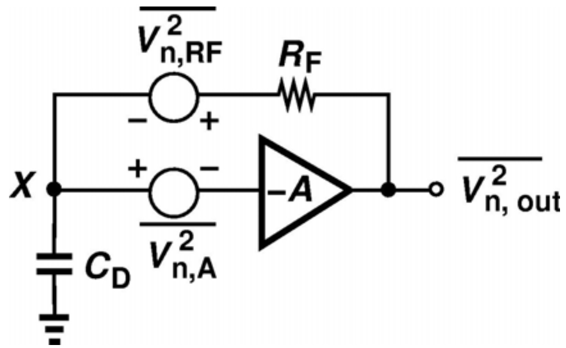


$$R_T = -\frac{AR_F}{A+1+R_F C_D s}$$

$$f_{-3dB} = \frac{A}{2\pi R_F C_D}$$

- R_F does not need to carry a bias current, relaxing the voltage headroom limitation.

Noise Performance of Feedback TIAs



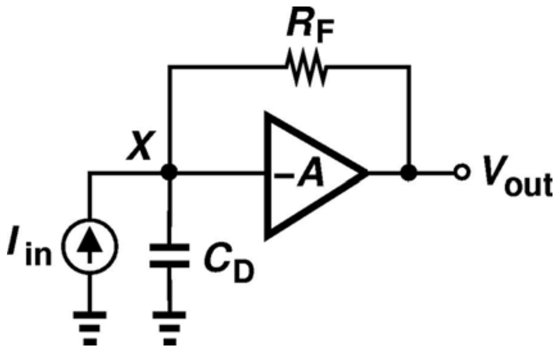
$$V_{n,out} = \frac{V_{n,RF} + (R_F C_D s + 1) V_{n,A}}{1 + R_F C_D s / A}$$

$$\overline{I^2_{n,in}} = \frac{4kT}{R_F} + \frac{\overline{V^2_{n,A}}}{R_F^2}$$

(when $C_D = 0$)

- Noise can be reduced by increasing R_F .
- $V_{n,RF}$ approaches $AV_{n,A}$ as the frequency goes to infinity $\Rightarrow$ inaccurate opamp model (it should have a finite bandwidth).

High Frequency Performance of Feedback TIAs



$$A(s) = \frac{A_0}{1 + s/\omega_0}$$

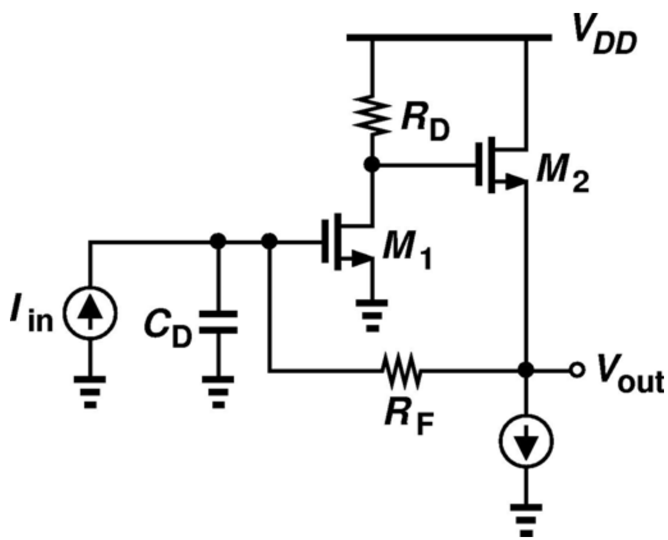
$$R_T = \frac{\dfrac{A_0\omega_0}{C_D}}{s^2 + \dfrac{R_F C_D + 1/\omega_0}{R_F C_D/\omega_0}s + \dfrac{(A_0+1)\omega_0}{R_F C_D}}$$

- **For maximum flatten response**

  $\Rightarrow \quad \zeta = \frac{1}{\sqrt{2}}, \quad f_{-3dB} = \frac{\sqrt{2}A_0}{2\pi R_F C_D}$

- **Bandwidth is greater than that of first order TIA by 41%.**

CMOS Realization of Feedback TIA



$$R_T = \frac{g_{m1}R_D}{1+g_{m1}R_D}R_F$$

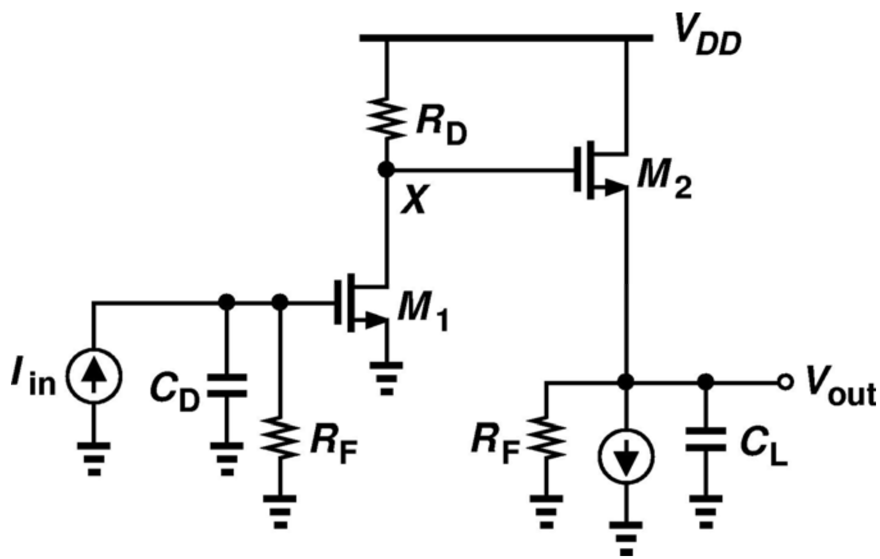
$$R_{in} = \frac{R_F}{1+g_{m1}R_D}$$

$$R_{out} = \frac{1/g_{m2}}{1+g_{m1}R_D}$$

$$\overline{I_{n,in}^2} = \frac{4kT}{R_F} + \frac{4kT}{R_F^2}\left(\frac{\gamma}{g_{m1}} + \frac{1}{g_{m1}^2 R_D} + \frac{\gamma}{g_{m2}g_{m1}^2 R_D^2}\right)$$

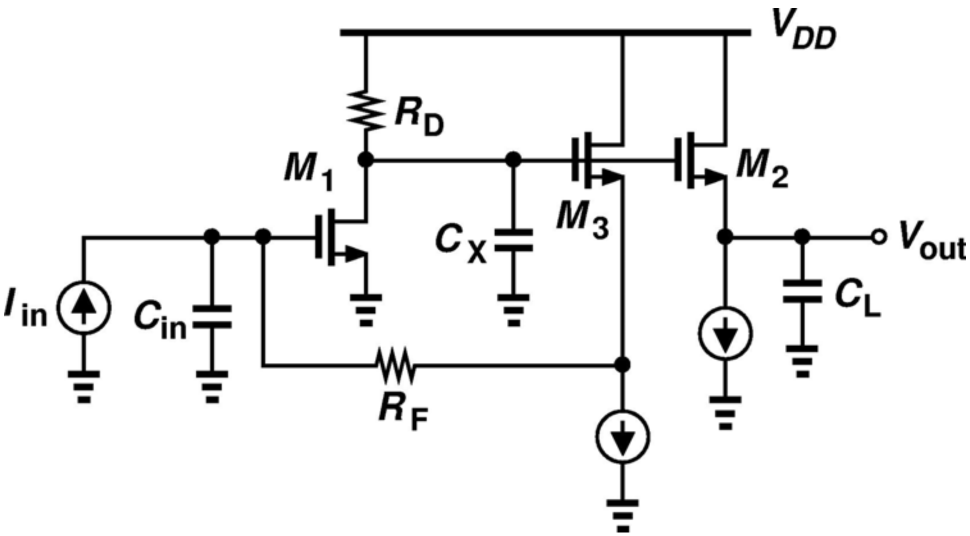
- Generally inversely proportional to R_F.

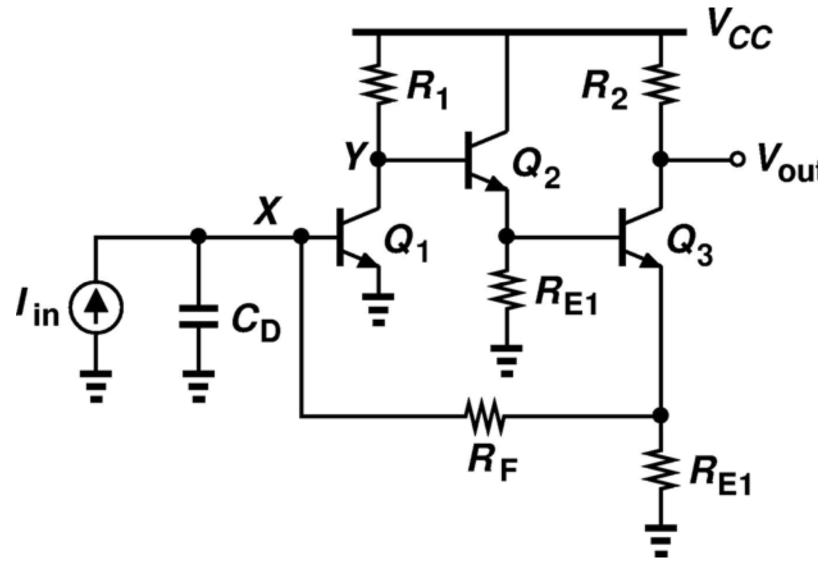
High-Frequency Behavior of Feedback TIA



- TIA may oscillate due to the three poles around the feedback loop.
- C_D and C_L are nontrivial.

Modified Feedback TIA

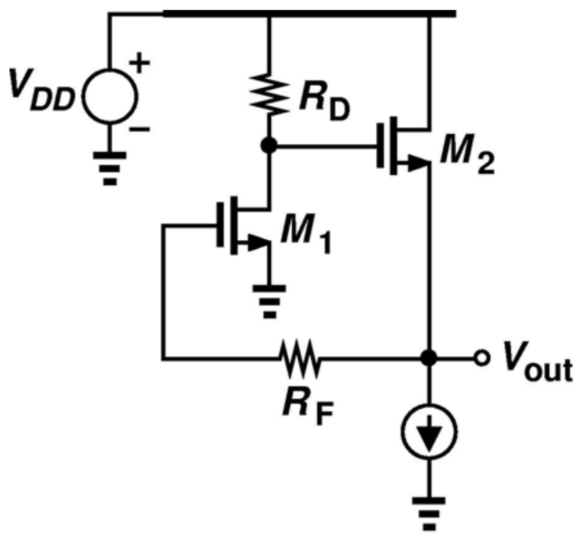




- Split the feedback loop with output port.
- Adding internal buffer.

Power Supply Rejection Issue

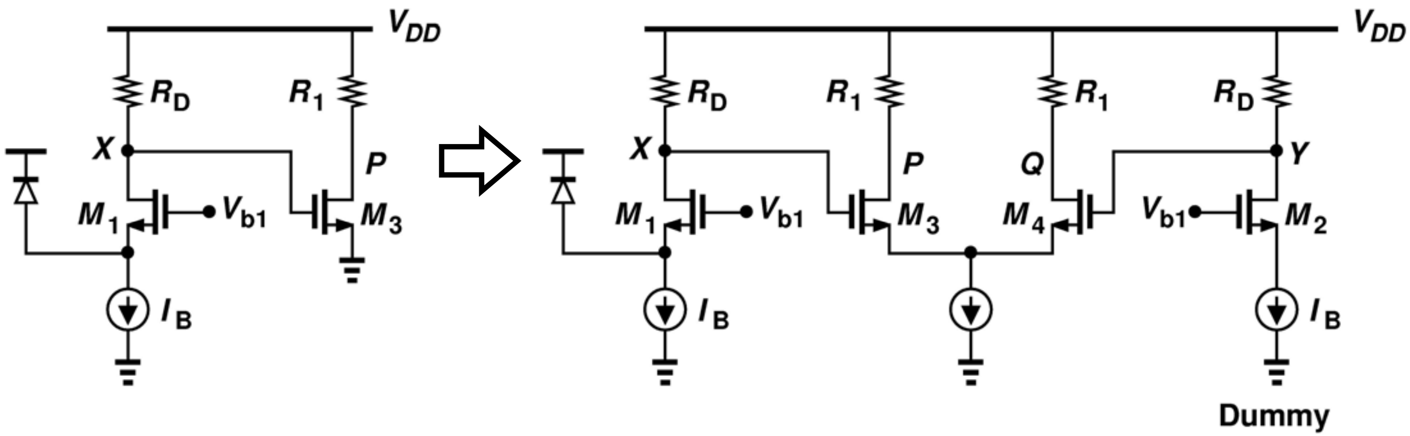
- Photodiode provides a single-ended current, leading to a single-ended TIA design and poor power supply rejection.

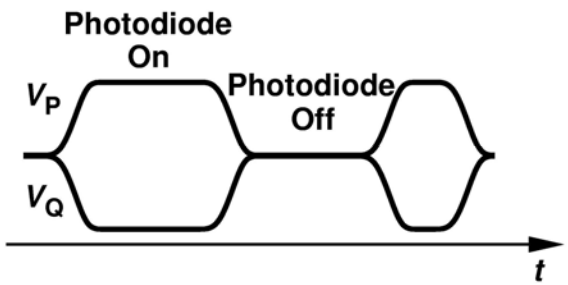


$$\frac{\partial V_{out}}{\partial V_{DD}} = \frac{1}{1 + g_{m1} R_D}$$

- Common issue for all single-ended circuits.

Differential TIAs



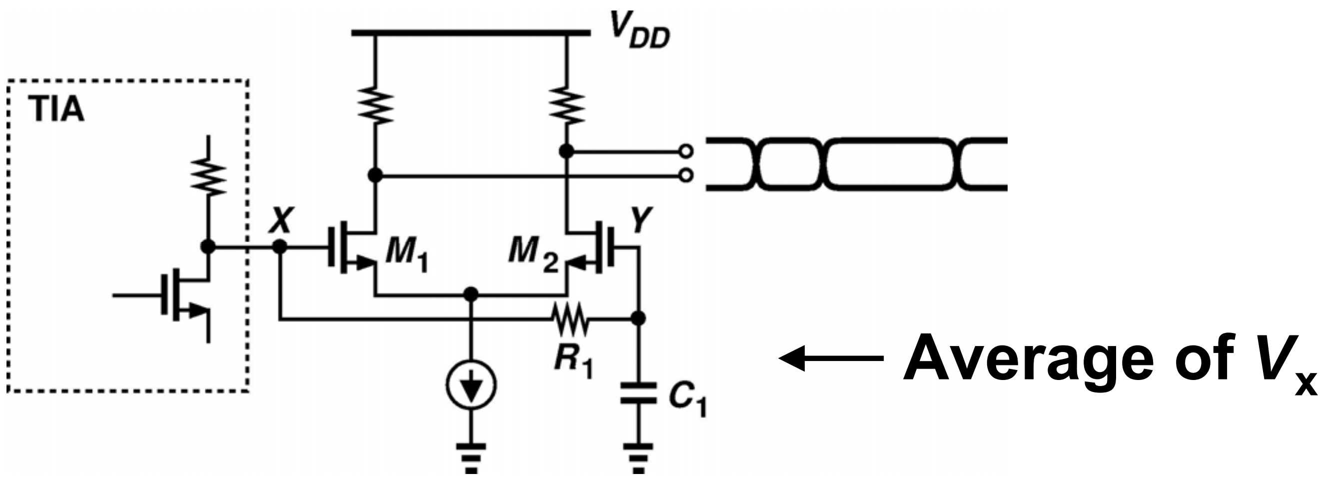


← "Pseudo" Differential

Issues:

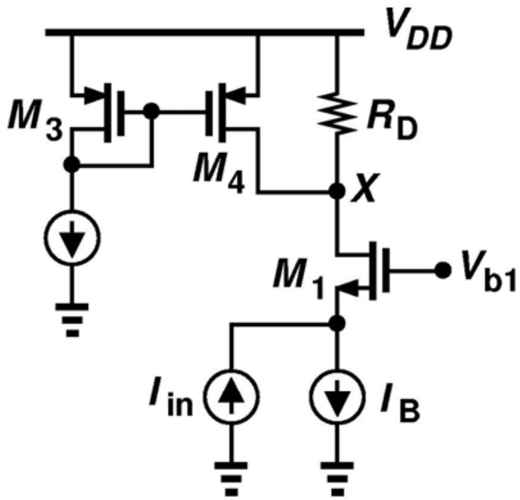
- Unequal gain and phase shift at high frequencies.
- Input noise current $\sqrt{2}$ times higher.
- Generating only "pseudo" differential output.

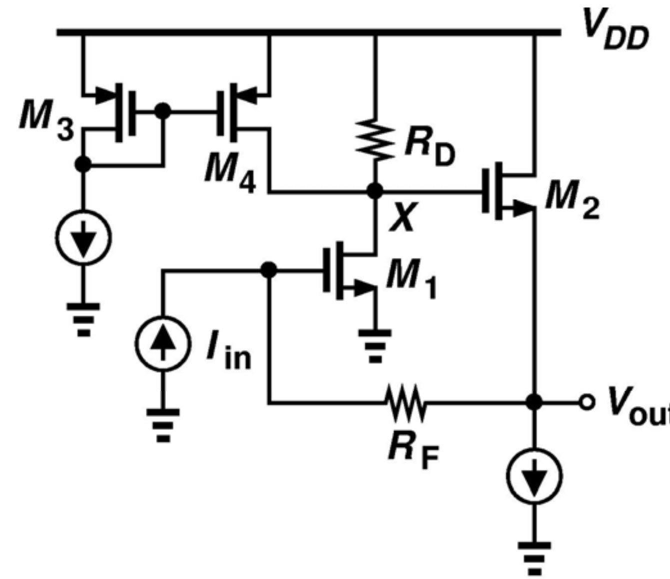
Single-Ended to Differential Conversion



- ❒ Time constant of tens of microseconds requires large external capacitor.
- ❒ Data pattern dependent.

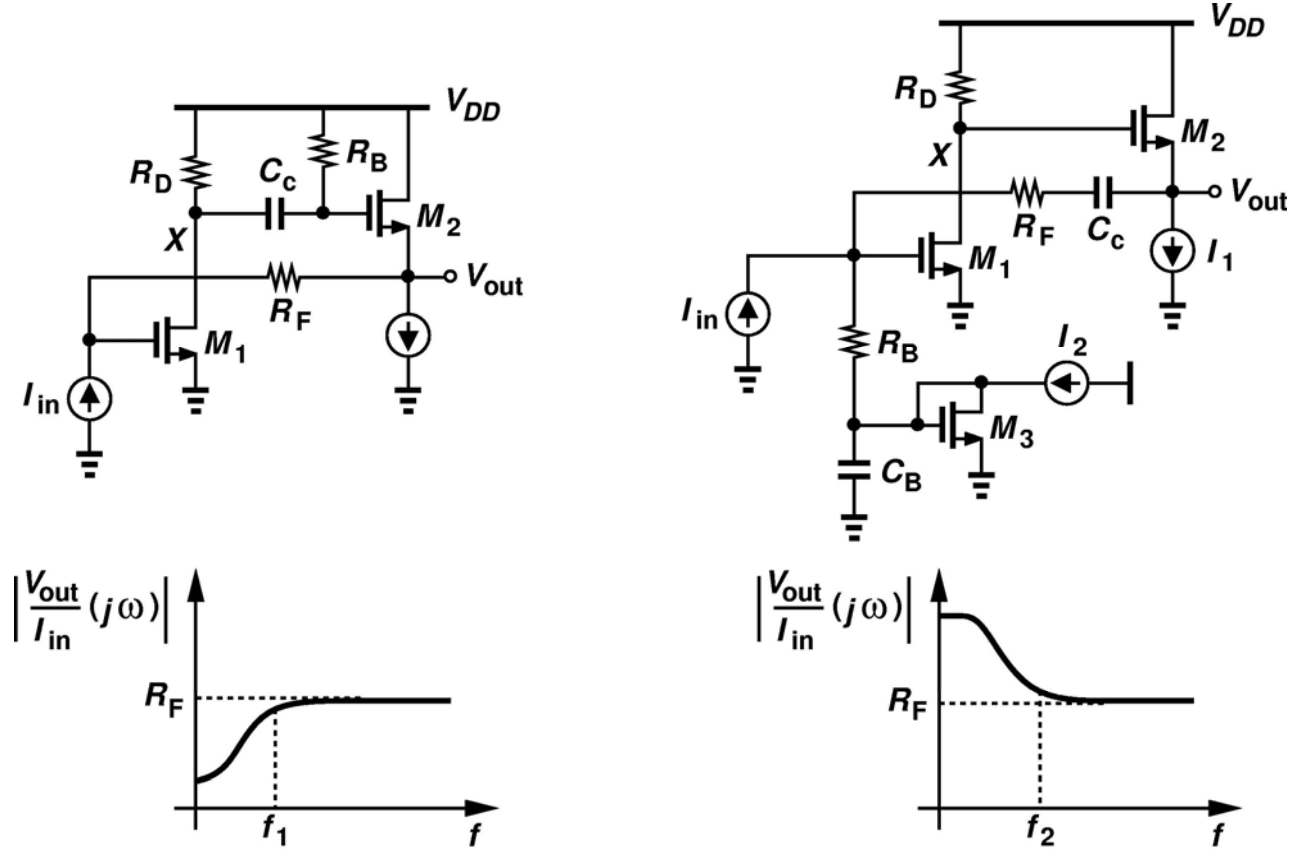
High-Gain Techniques





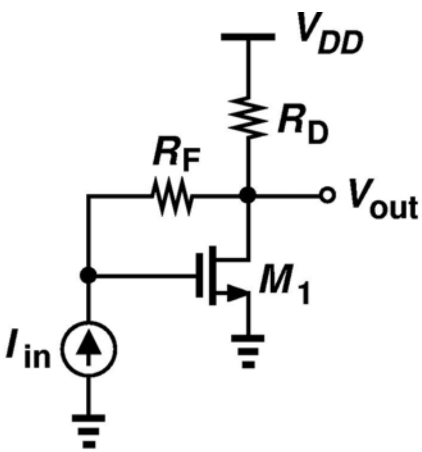
- ❐ **Providing extra current without IR drop.**
- ❐ **Noise inevitably becomes higher.**
  (Under what condition?)

Capacitive Coupling



- Relax the voltage-headroom requirement.
- Some standards need very long runs, leading to external large *R* and *C*.
- Stability is of concern.

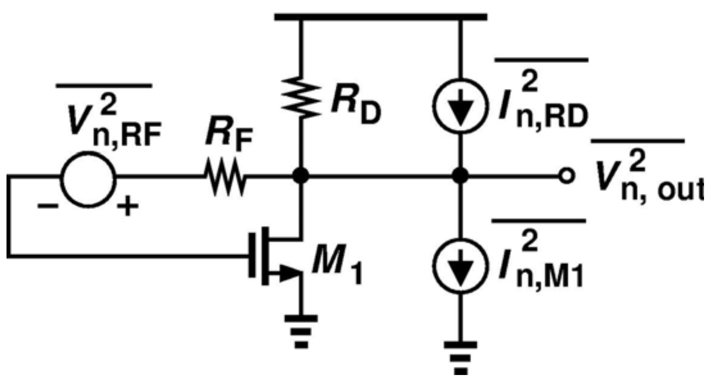
Feedback TIA without Source Follower



$$\frac{V_{out}}{V_{in}} = -\frac{g_m R_F - 1}{g_m R_D + 1} R_D \approx -R_F$$

$$R_{in} = \frac{R_F + R_D}{g_m R_D + 1}$$

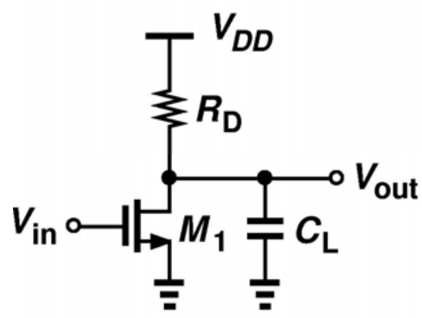
$$R_{out} = R_D \| \frac{1}{g_m}$$

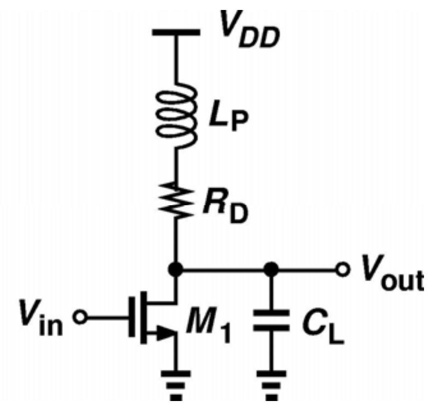


$$\overline{I^2_{n,in}} = \frac{4kT\gamma}{g_m R_F^2} + \frac{4kT}{g_m^2 R_F^2 R_D} + \frac{4kT}{R_F}$$

- Degenerate the source follower.
- Tradeoffs between gain, stability, noise, and robustness.

Inductive Peaking



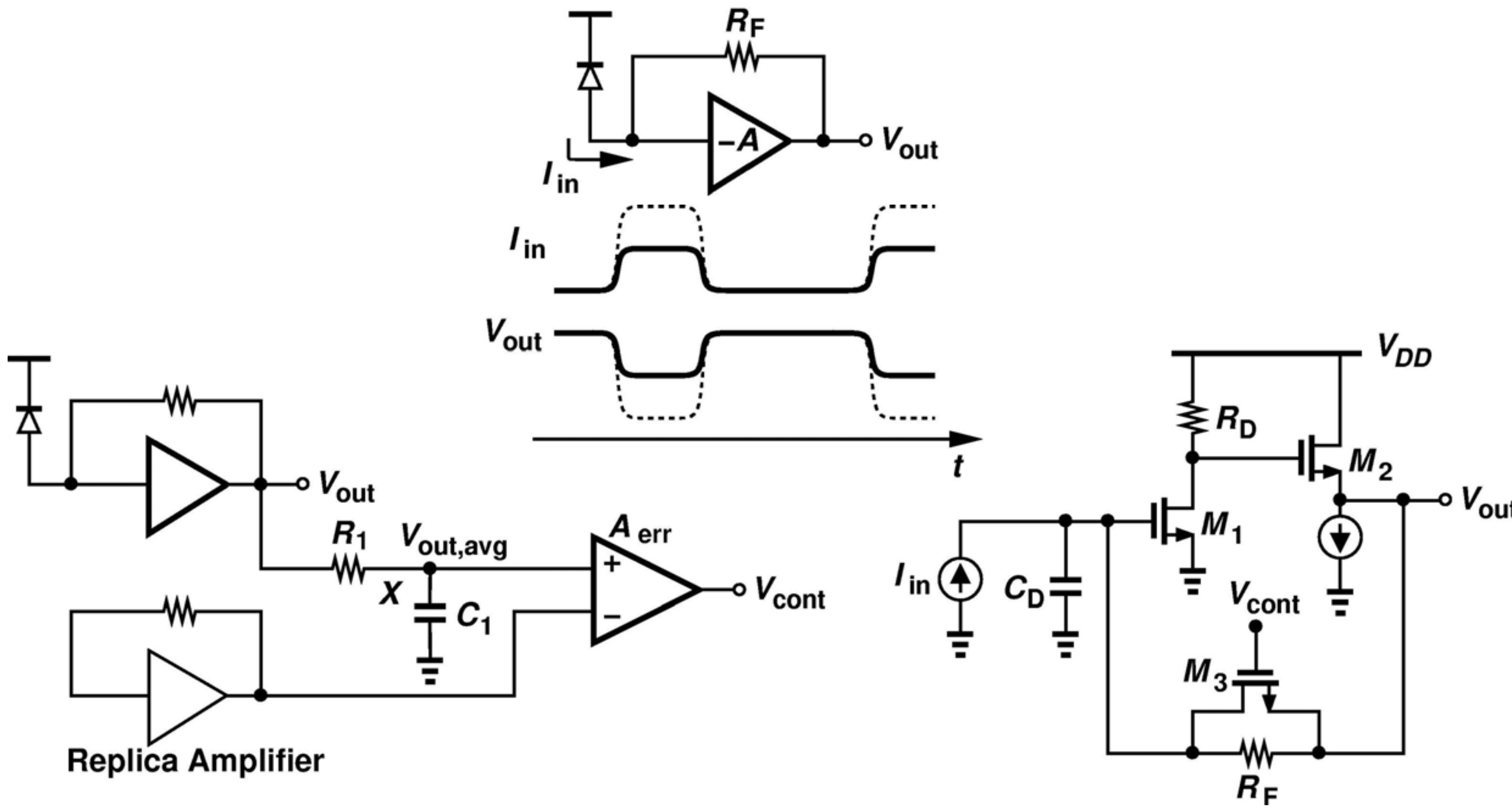


$$f_{-3dB} = \frac{1}{2\pi R_D C_L}$$

$$\frac{V_{out}}{V_{in}} = -g_m R_D \frac{s + 2\zeta\omega_n}{s^2 + 2\zeta\omega_n + \omega_n^2} \frac{\omega_n}{2\pi}$$

$$f_{-3dB} = \frac{1.79}{2\pi R_D C_L} \quad \text{for } \zeta = 1/\sqrt{2}$$

Automatic Gain Control



- Large input current may degrade the response be pulling one or more current source into triode region.
- Necessitating dynamic tracking mechanism to adjust it in real time.

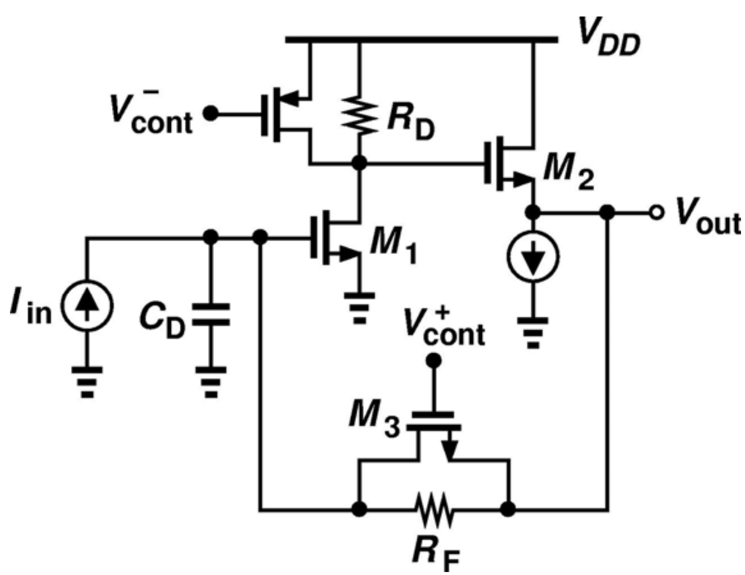
Automatic Gain Control

- Since

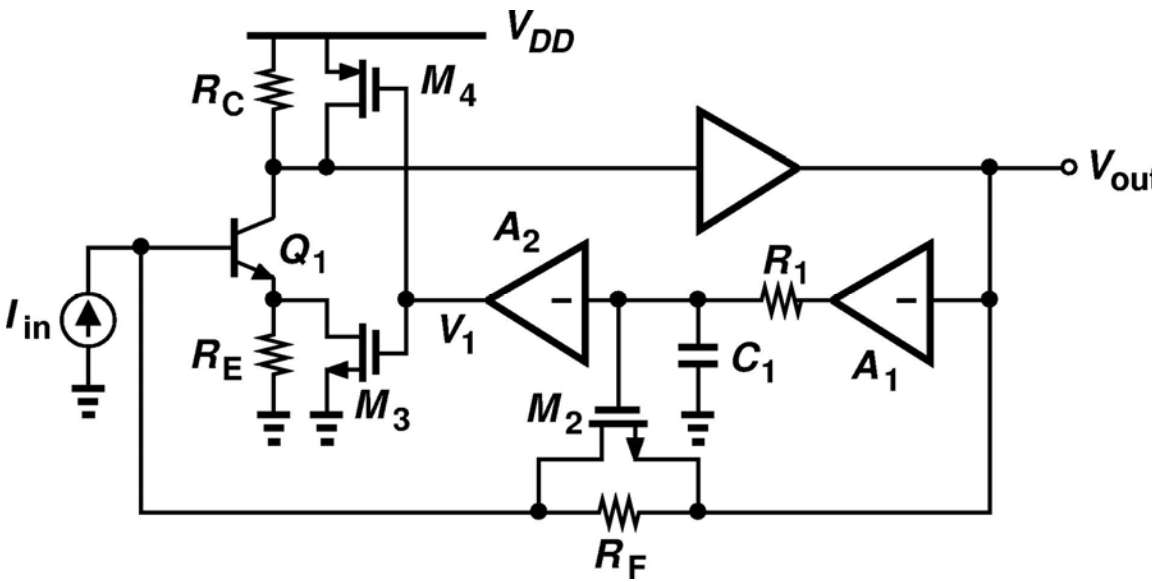
$$\zeta = \frac{1}{2}\sqrt{\frac{R_F C_D \omega_0}{A_0 + 1}}$$

system may become unstable as R_F goes down.

$\Rightarrow$ Need to reduce A_0 so as to maintain a relatively constant ζ.

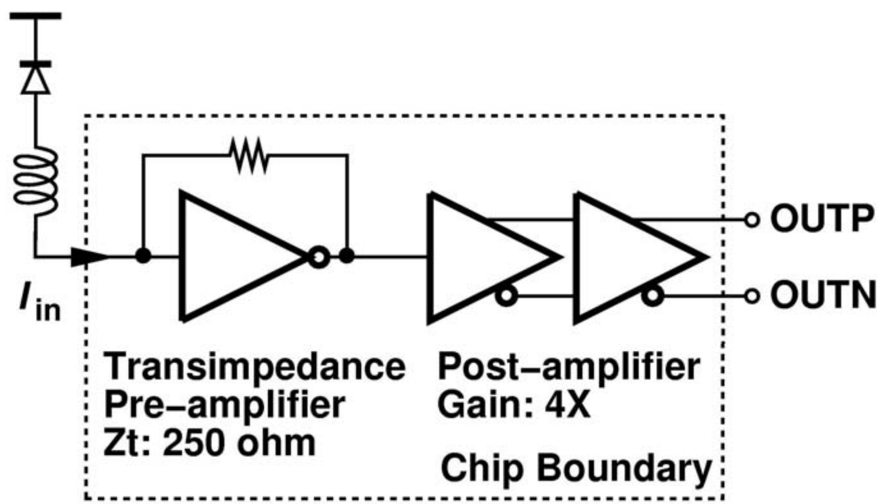


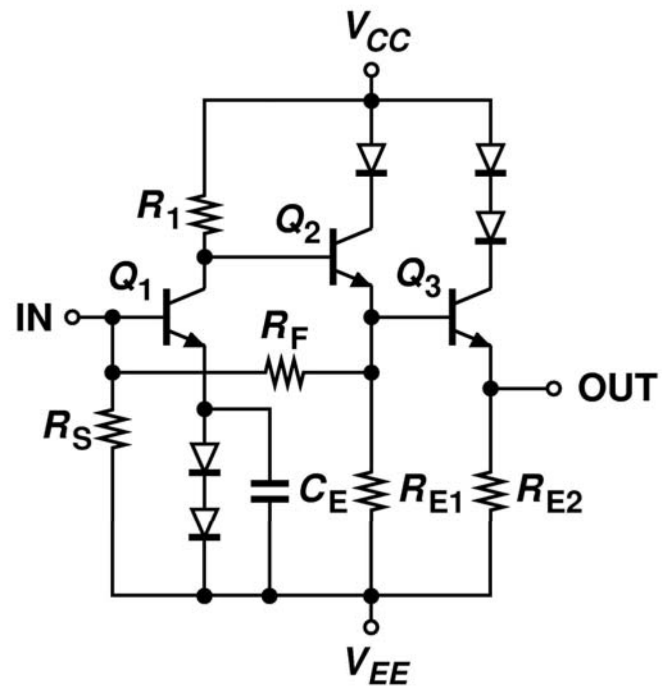
Case Study (I)



Korramabadi et. al. [ISSCC, 96]

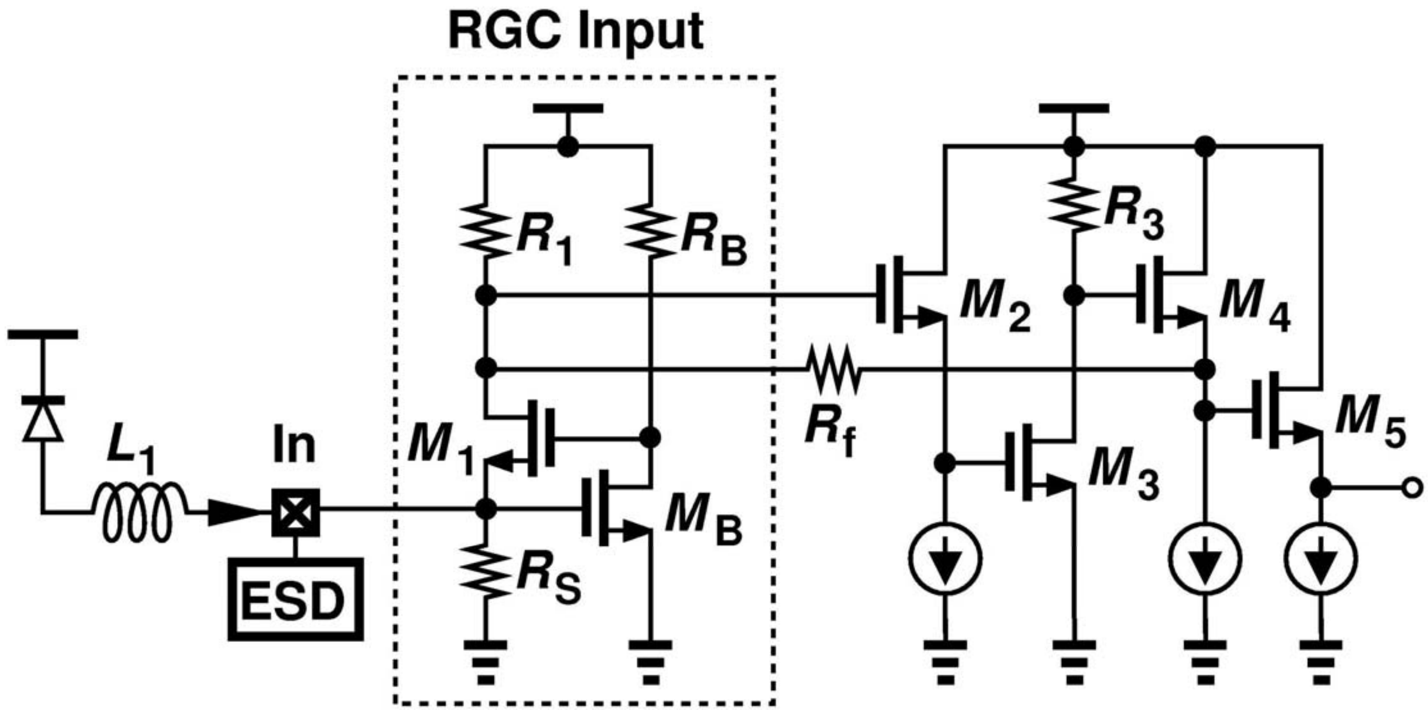
Case Study (II)





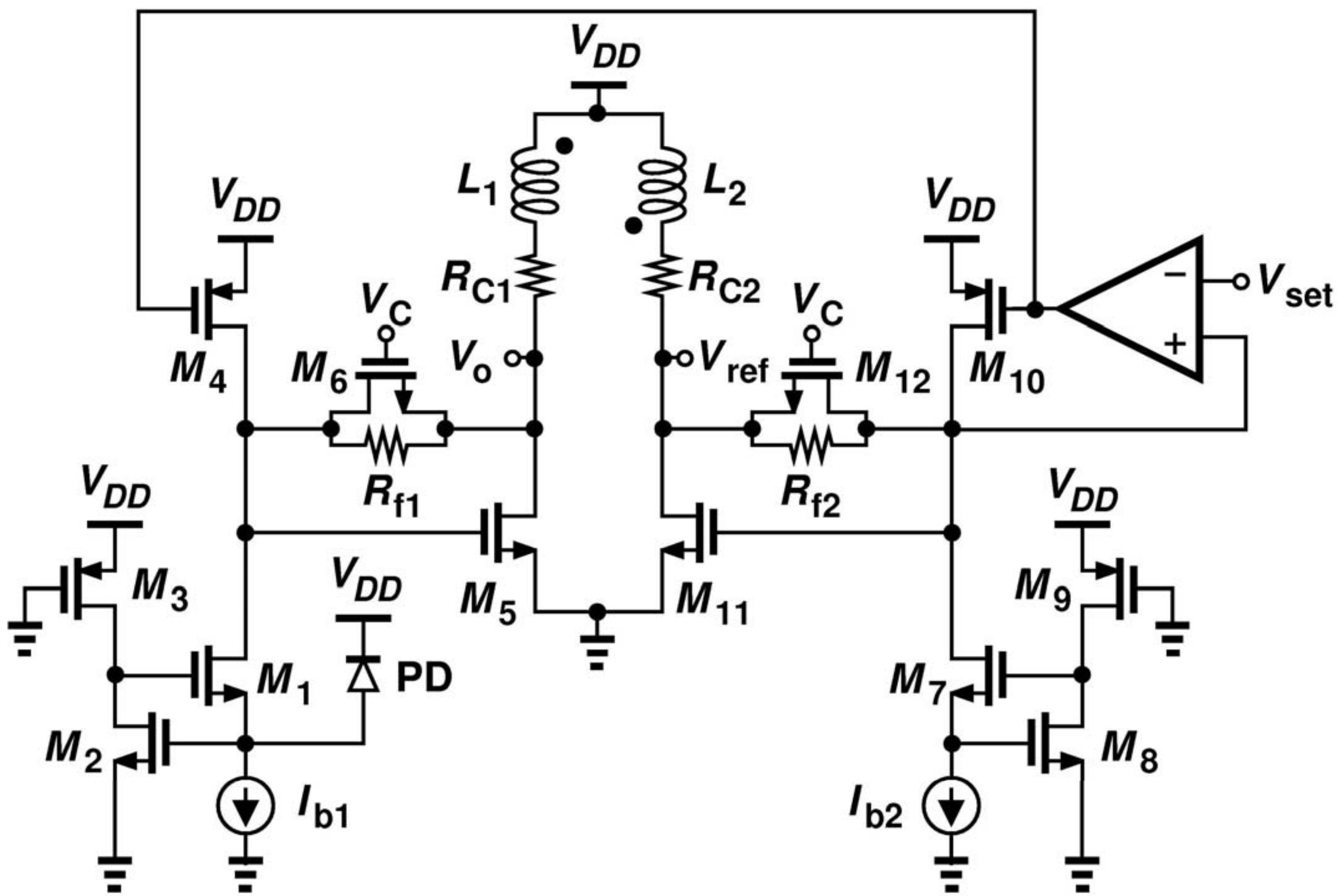
Wu et. al. [JSSC, 03]

Case Study (III)



Park et. al. [JSSC, 04]

Case Study (IV)

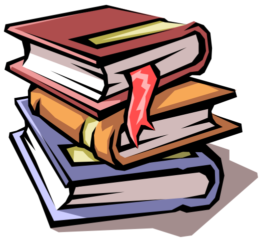


Chen et. al. [JSSC, 05]

Limiting Amplifiers

Professor Jri Lee

台大電子所　李致毅教授

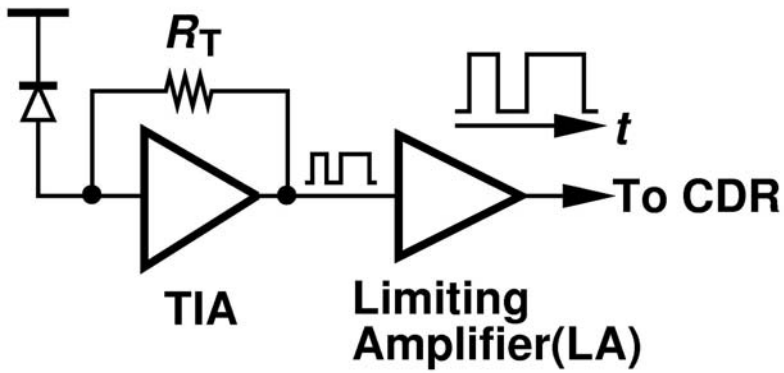


Electrical Engineering Department
National Taiwan University

Outline

- Introduction
- Design Challenges
- Loss of Signal Detection
- Broadband Techniques
- Case Study

General Considerations



- **Requirement**

  High Gain (40~60dB)

  Broad Bandwidth ($\geq$ 0.7 $\times$ Data Rate)

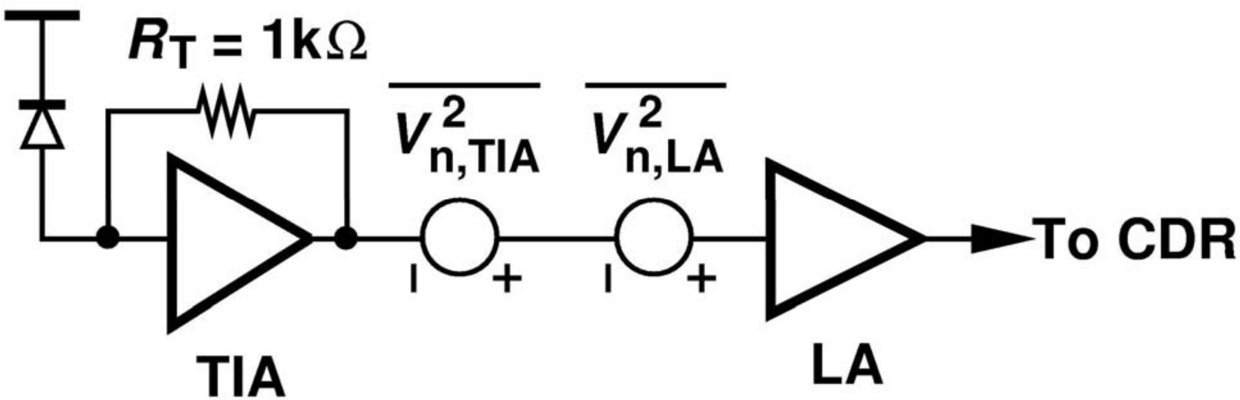
  Low Noise (300 ~ 400 μV_{rms})

  Small Offset Voltage

  Well-Behaved Response to Large Signals

Challenges of Noise

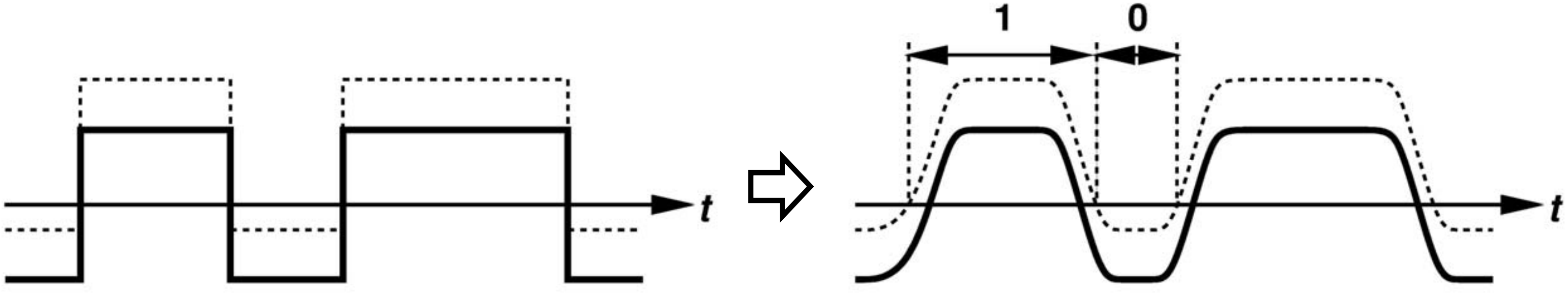
Example: OC-192 Receiver (Data Rate $\approx$ 10Gb/s)



- For TIA output noise = 1 mV_{rms} and LA contributes 10% of noise ⇨ LA input noise = 330 μV_{rms}
- For a bandwidth of 10 GHz ⇨ $V_{n,LA}$ < 3 $nV/\sqrt{Hz}$

Offset Due to Mismatches

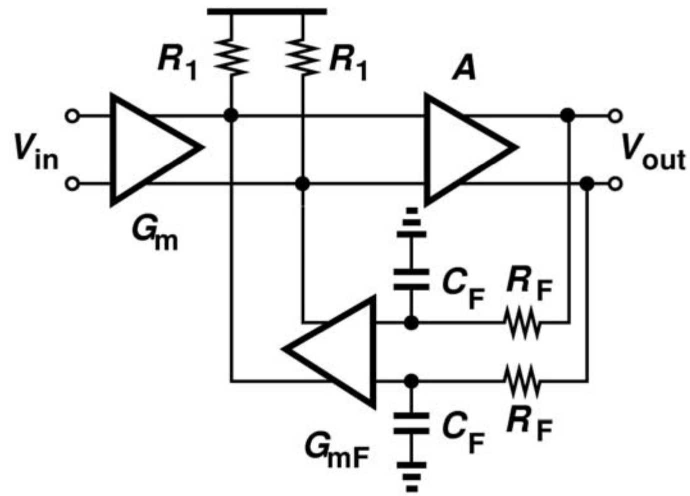
- Random asymmetries (e.g., device mismatches) in LA result in finite offset.
- Offset degrades sensitivity and causes pulse-width distortion, necessitating cancellation technique.
- Offset may totally destroy the output in high-gain systems (Why?).



Ideal Pulses

Pulses with Finite Rise/Fall Time

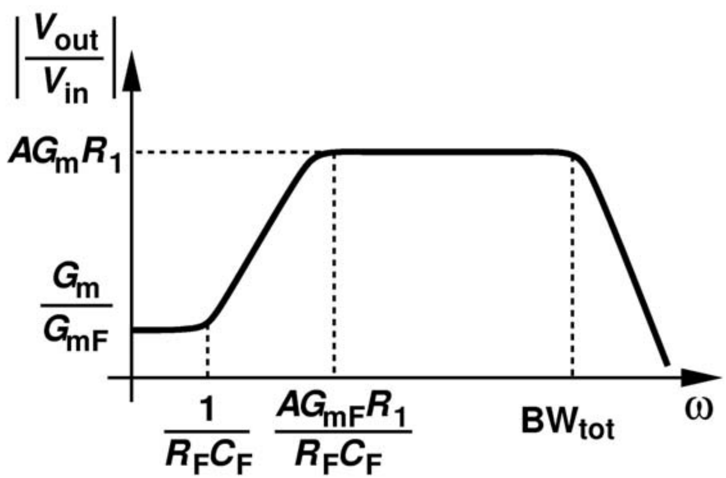
Offset Cancellation Technique



$$[V_{os,in} - V_{os,out} G_{mF} R_1] A = V_{os,out}$$

$$V_{os,out} = \frac{A}{1 + A G_{mF} R_1} V_{os,in}$$

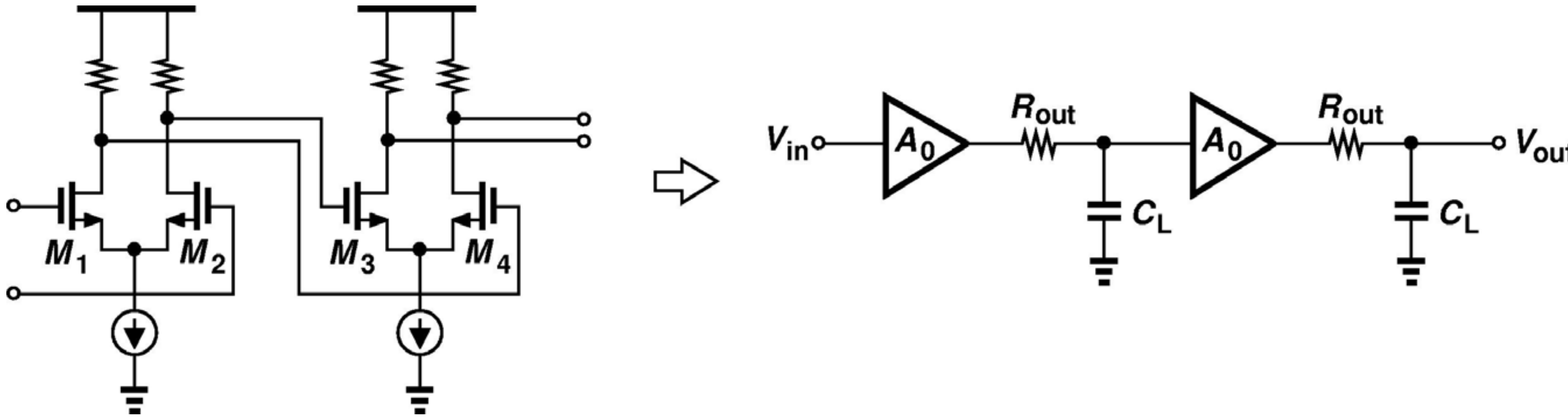
$$\approx \frac{V_{os,in}}{G_{mF} R_1}$$



$$\frac{V_{out}}{V_{in}} = \frac{A G_m R_1 (1 + s C_F R_F)}{1 + A G_{mF} R_1 + s C_F R_F}$$

- Offset cancellation introduces one zero and one pole.
- Lower corner defined by standards, usually very low.

First Order Realization of Gain Stages



$$\omega_0 = \frac{1}{R_{out} C_L}$$

$$BW_{tot} = \omega_0 \sqrt{2^{1/n} - 1}$$

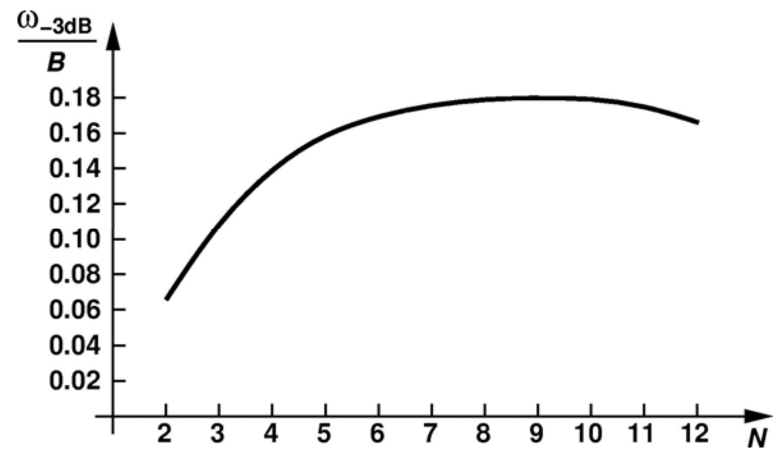
- Cascading identical amplifying stages.
- Trade bandwidth with gain since the latter increases in a way faster than the former decreases.

Optimization of Stage Numbers

- For a given technology, the gain-bandwidth product is relatively constant.

$$\Rightarrow BW_{tot} = \frac{GBW}{A_{tot}^{1/n}} \sqrt{2^{1/n} - 1}$$

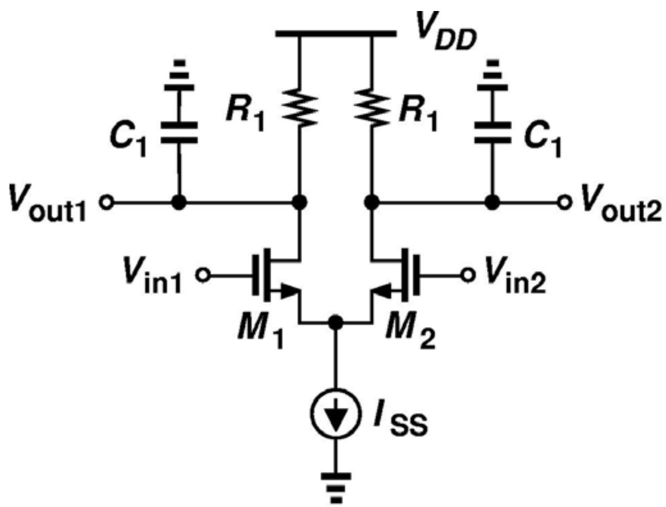
$$\Rightarrow n_{opt} = 2 \ln A_{tot}$$

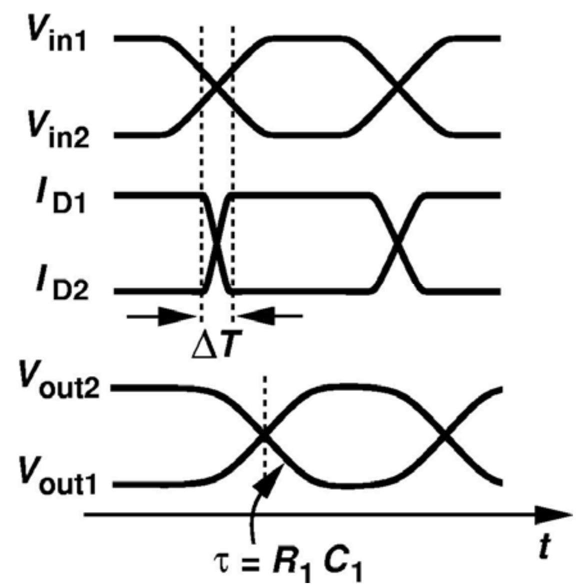


- For A_{tot} = 50 dB, n_{opt} = 11
- However, noise and power issues limit the number of stage to 5.

Large Swing Effect

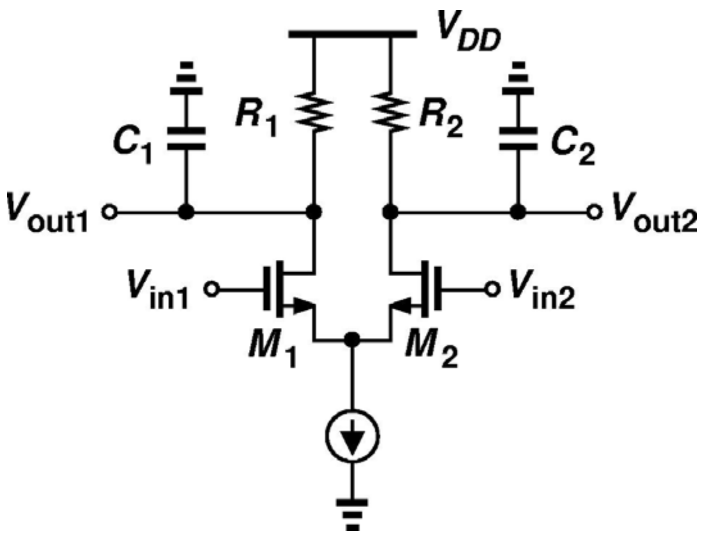
- Small-signal gain-bandwidth analysis is pessimistic!





- The last few stages switch with large input.
  - $\Rightarrow$ The speed of a cascade of stages is limited by only that of one stage.

AM/PM Conversion

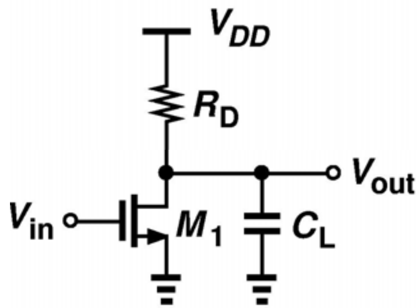


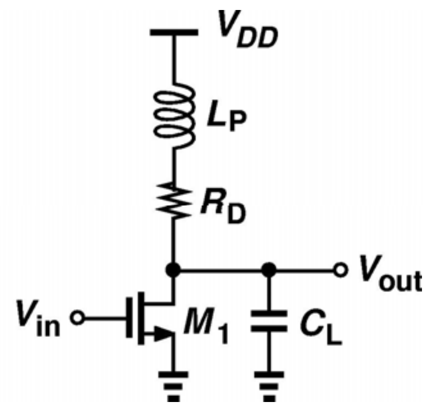
$$I_{out} = \alpha_1 V_{in} + \alpha_3 V_{in}^3$$

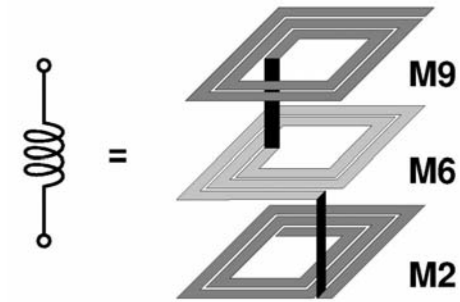
$$V_{out}(t) = A_1(\alpha_1 V_m + \frac{3}{4}\alpha_3 V_m^3)\sin(\omega t + \theta_1) - A_3 \frac{3}{4}\alpha_3 V_m^3 \sin(3\omega t + \theta_2)$$

- Noise on input signal amplitudes translates to variations of output zero crossings, i.e., jitter.

Broadband Technique (I): Inductive Peaking







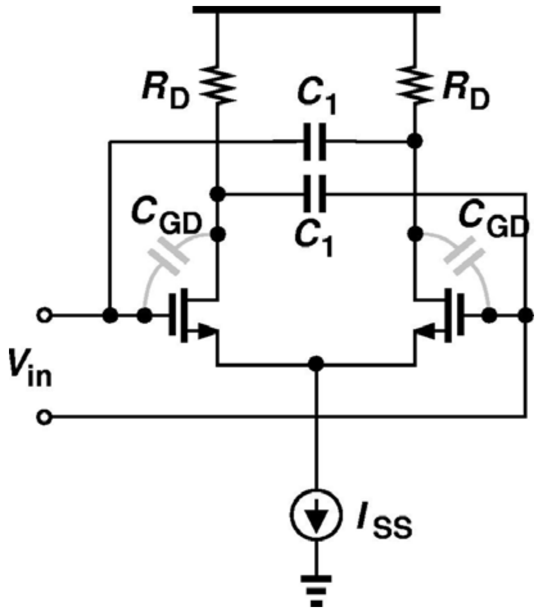
$$f_{-3dB} = \frac{1}{2\pi R_D C_L}$$

$$\frac{V_{out}}{V_{in}} = -g_m R_D \frac{s + 2\zeta\omega_n}{s^2 + 2\zeta\omega_n s + \omega_n^2} \frac{\omega_n}{2\zeta}$$

$$f_{-3dB} = \frac{1.79}{2\pi R_D C_L} \quad \text{for} \quad \zeta = 1/\sqrt{2}$$

- ❒ **Most Efficient method; no extra power consumption.**
- ❒ **Area consuming (although has been moderated in advanced technology).**

Broadband Technique (II): Miller Capacitor Cancellation



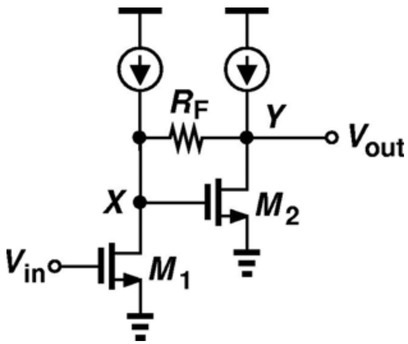
$$C_{GD,eff} = (1 + g_m R_D) C_{GD}$$

$$C_{1,eff} = (1 - g_m R_D) C_1$$

$$\Rightarrow C_1 = \frac{g_m R_D + 1}{g_m R_D - 1} C_{GD} \approx C_{GD}$$

- Mismatch or process variation matters.
- Efficient only for high gain.
- Button-plate parasitics degrade the performance.

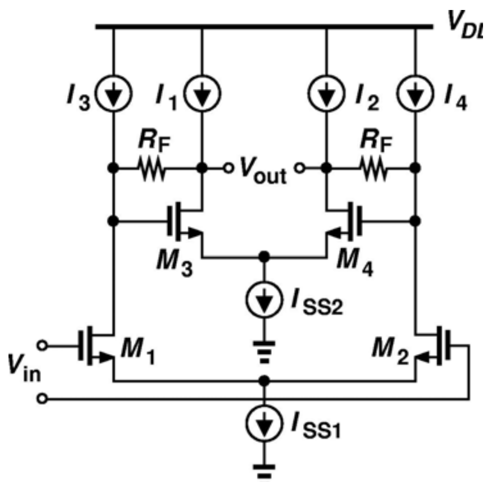
Broadband Technique (III): Cherry-Hooper Amplifiers

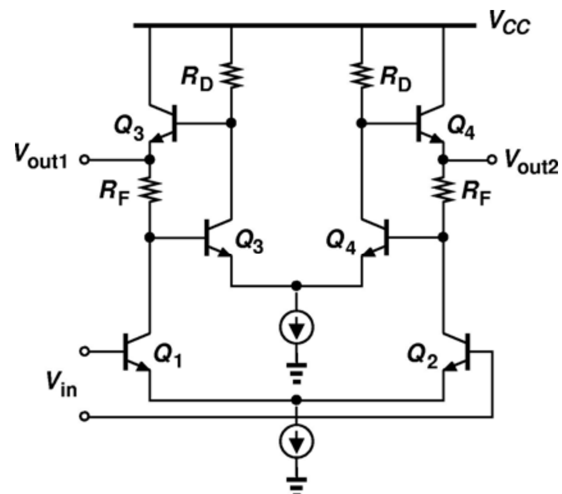


$$\frac{V_{out}}{V_{in}} = g_{m1}R_F - \frac{g_{m1}}{g_{m2}}$$

$$\omega_{p,X} \approx \frac{g_{m2}}{C_X}$$

$$\omega_{p,Y} \approx \frac{g_{m2}}{C_Y}$$

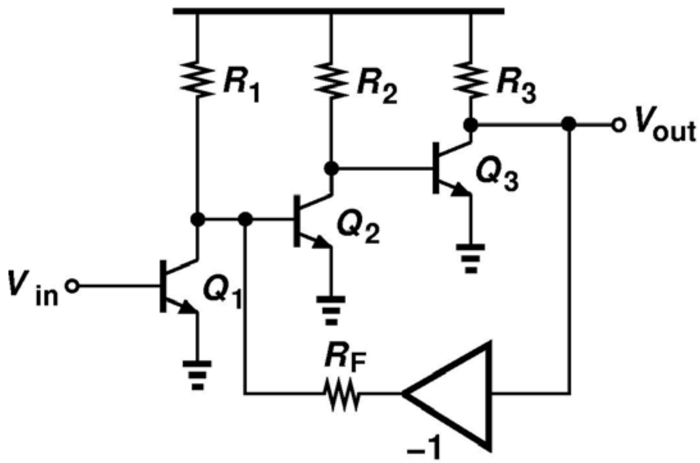




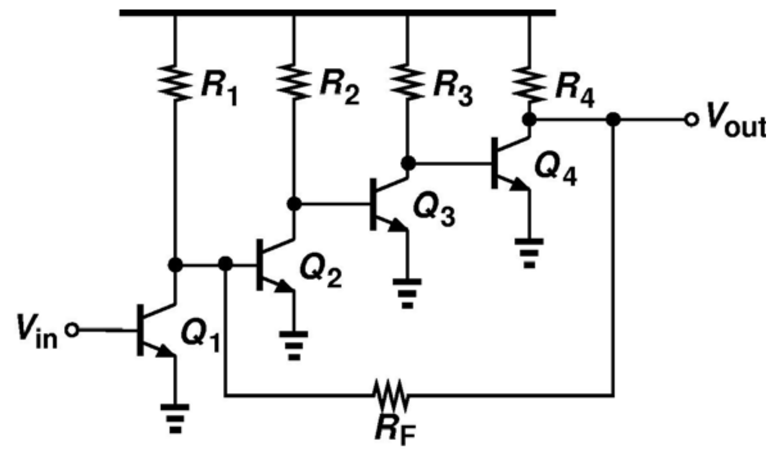
- ❐ Increase the bandwidth significantly in a cost of minor gain loss.
- ❐ Voltage headroom might be an issue in low supply technologies.

Broadband Techniques (IV): Voltage-Current Feedback

- Voltage-current (shunt-shunt) feedback can be further applied to multiple stages.
- Watch level shifting in BJT.

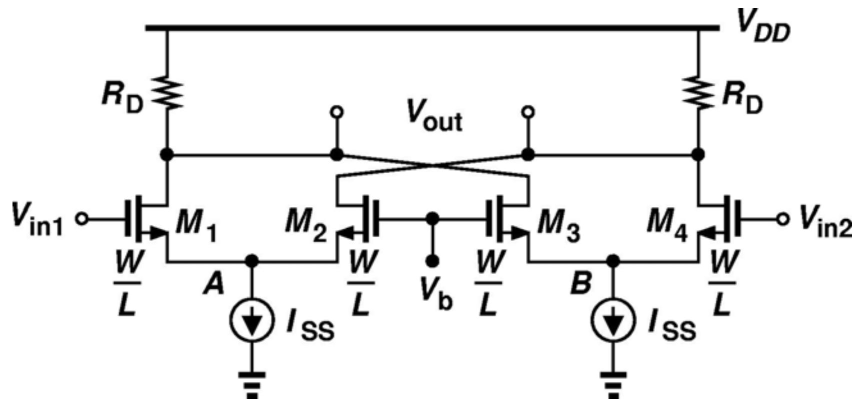


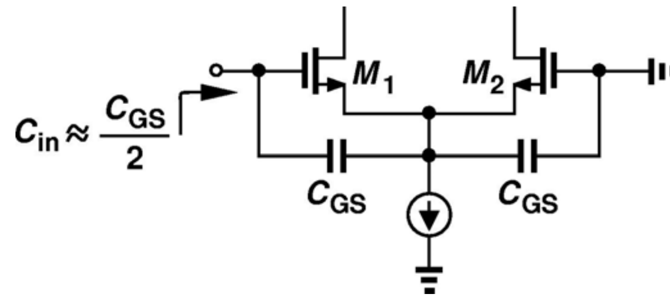
Double



Triple

Broadband Techniques (V): f_T Doubler

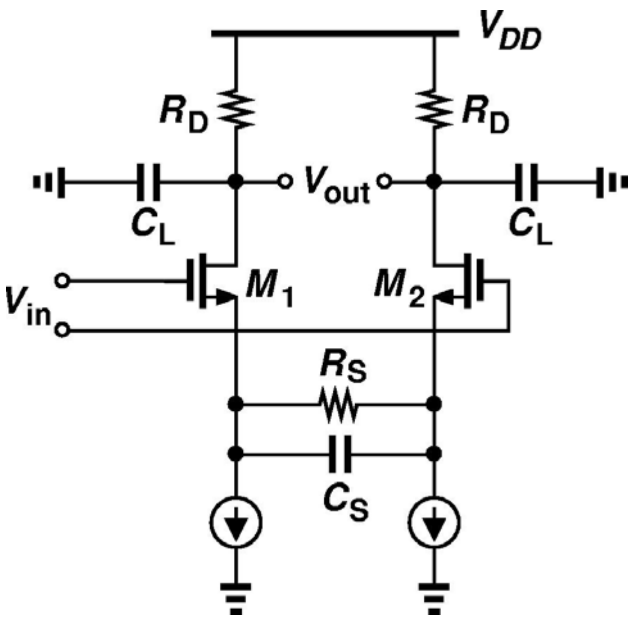




$$V_{out} = g_m (V_{in1} - V_{in2}) R_D$$

- Double IR drop, voltage headroom issue.
- Parasitics on tail current sources degrade the performance.
- Still quite useful in output buffer designs.

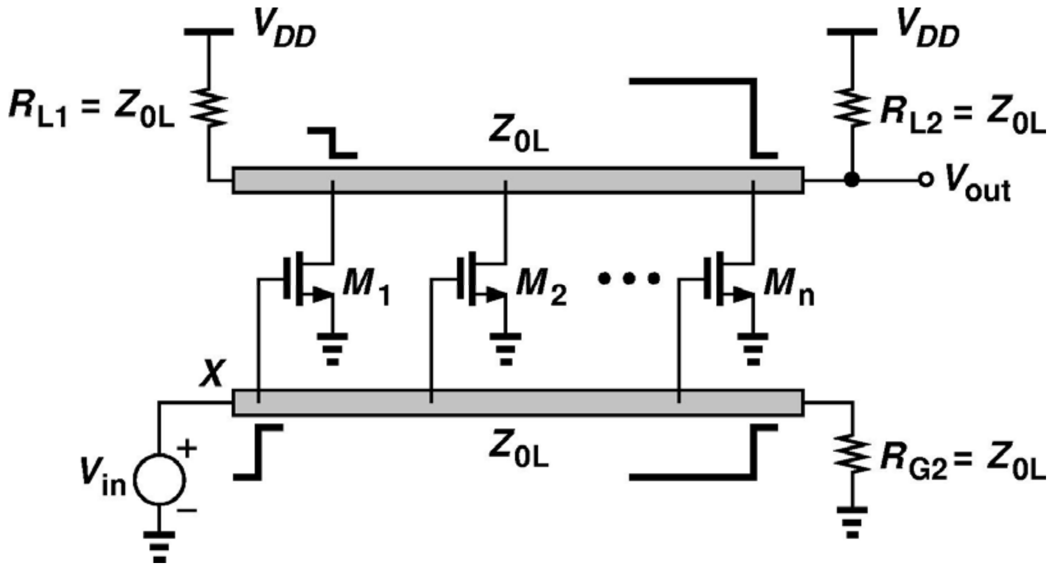
Broadband Technique (VI): Capacitive Degeneration



$$\frac{V_{out}}{V_{in}} = \frac{g_m(1+R_sC_s s)}{R_sC_s s+1+\dfrac{g_mR_s}{2}}\frac{R_D}{1+sC_LR_D}$$

- If $R_S C_S = R_D C_L$, bandwidth increases by a factor of $(1+g_m R_S/2)$ whereas gain decreases by the same amount.

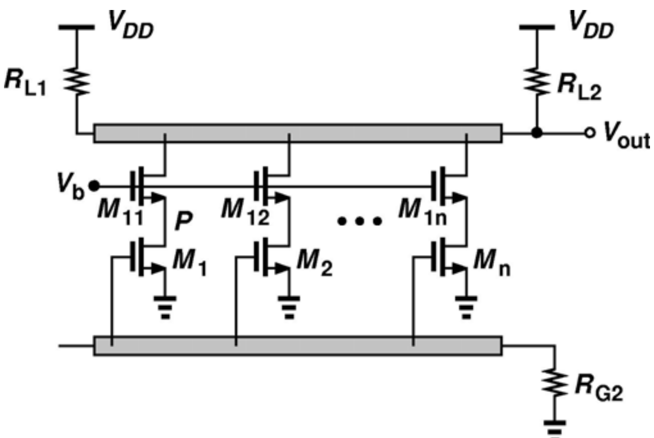
Broadband Technique (VII): Distributed Amplification

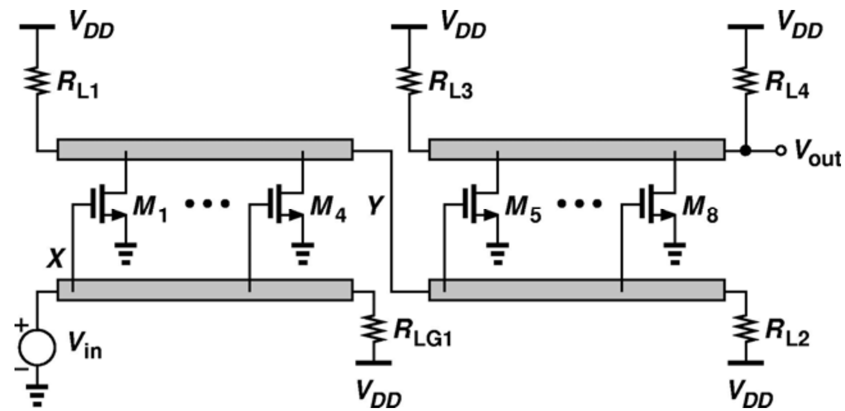


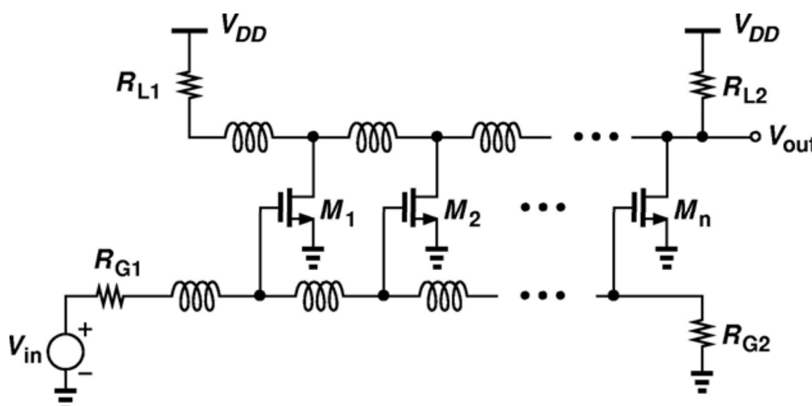
$$A_v = g_m \frac{Z_{0L}}{2} n \approx \pi f_T \frac{l}{v}$$

- Voltage gain is proportional to physical length *l*.
- With ideal T-lines, distributed amplifiers would achieve infinite gain with infinite bandwidth!

Modified Distributed Amplifiers

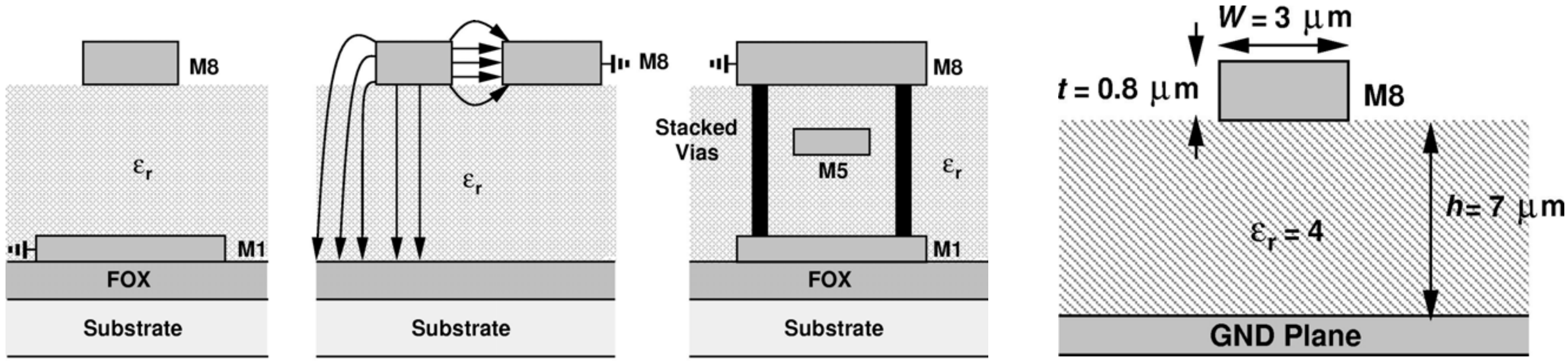






- Cascade and segmented structure helps to improve the performance.

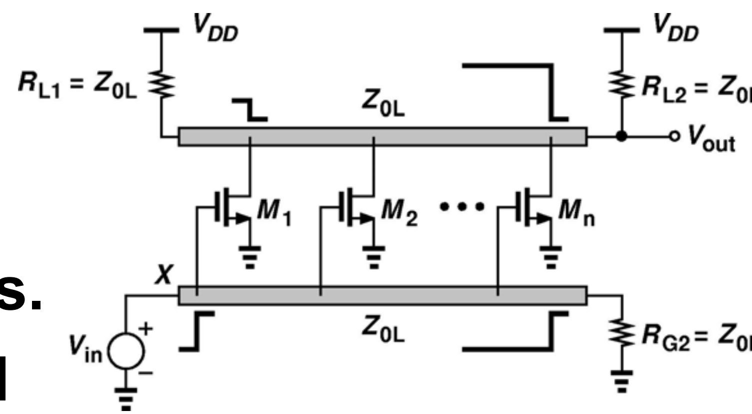
Realization of Monolithic Transmission Lines



- mm-wave techniques become practical in deep-submicron CMOS.
- T-lines are lossy but still useful.

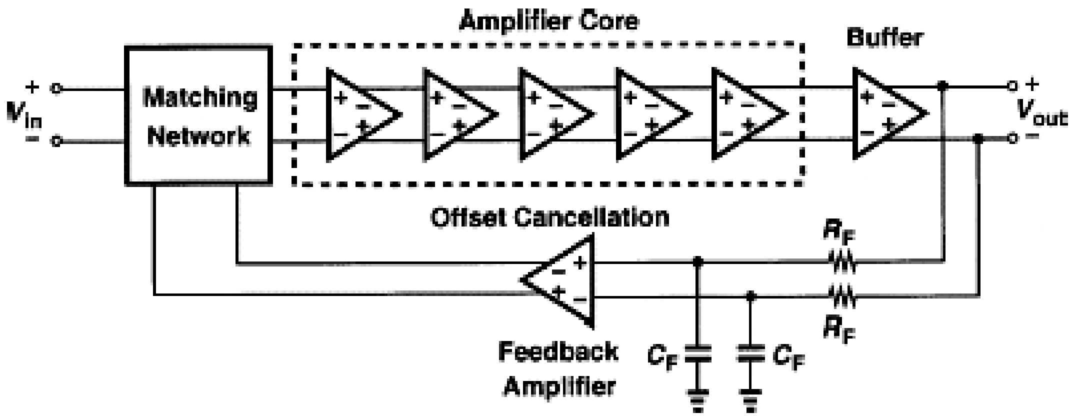
Challenges of Distributed Amplifiers

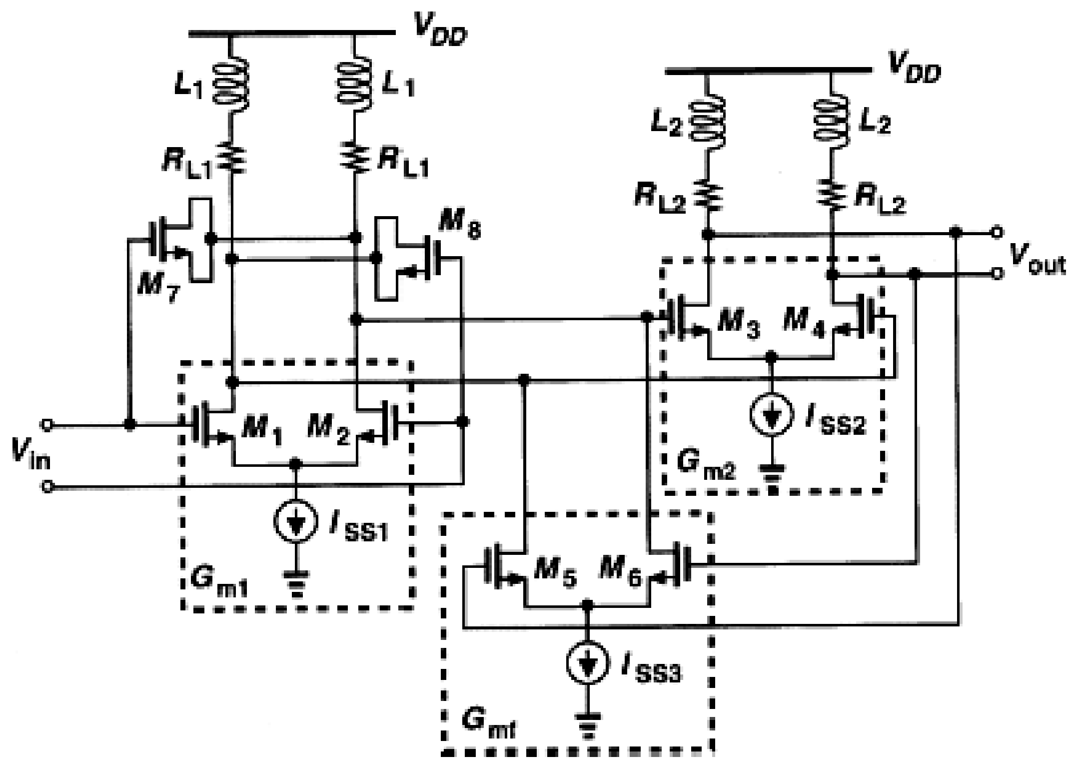
- Transmission Line Loss.
- Output resistance of transistors.
- Miller capacitance.
- Propagation velocity mismatches.
- Routing difficulties in differential realization.
- PVT variations.

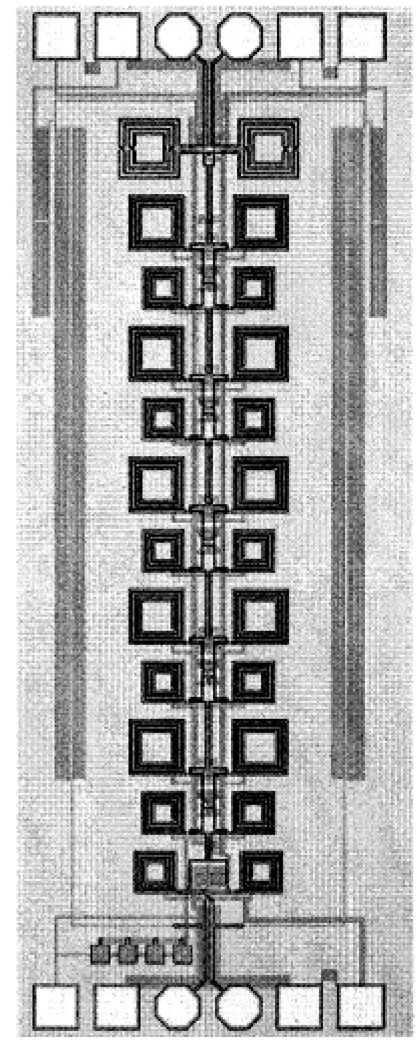


⇒ Nevertheless, T-line based distributed amplifiers still provide promising applications.

Case Study





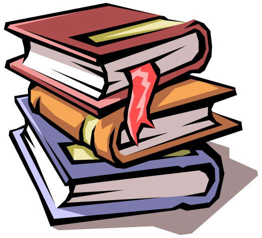


[Galal et al., 2003]

Equalizers

Professor Jri Lee

台大電子所　李致毅教授



Electrical Engineering Department

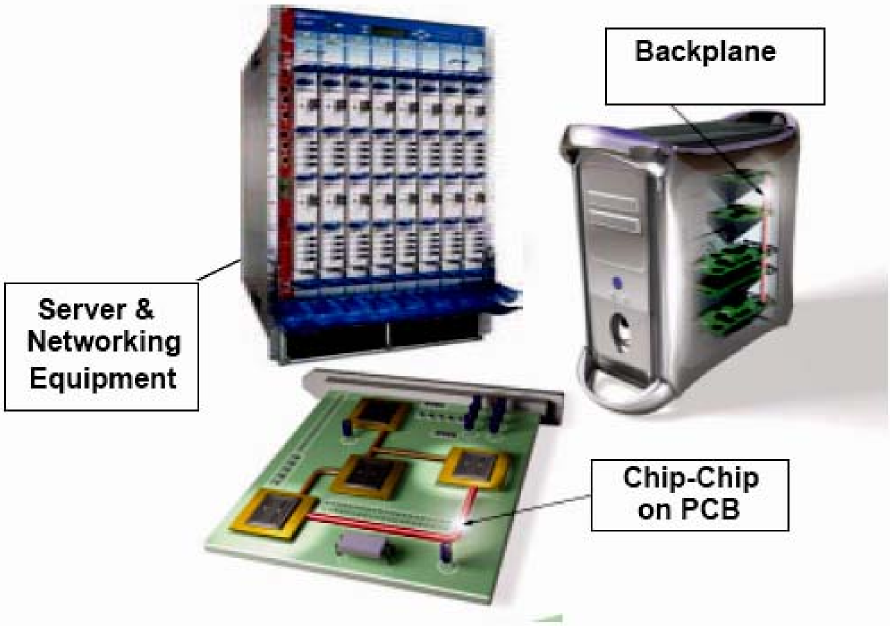
National Taiwan University

Outline

- Introduction
- Pre-Emphasis and Drivers
- Post-Emphasis and Equalizers
- Design of Building Blocks
- Case Study

Reference: “Digital Communications” by John Proakis (4th Edition).

High-Speed Data Transfer (Electrical)

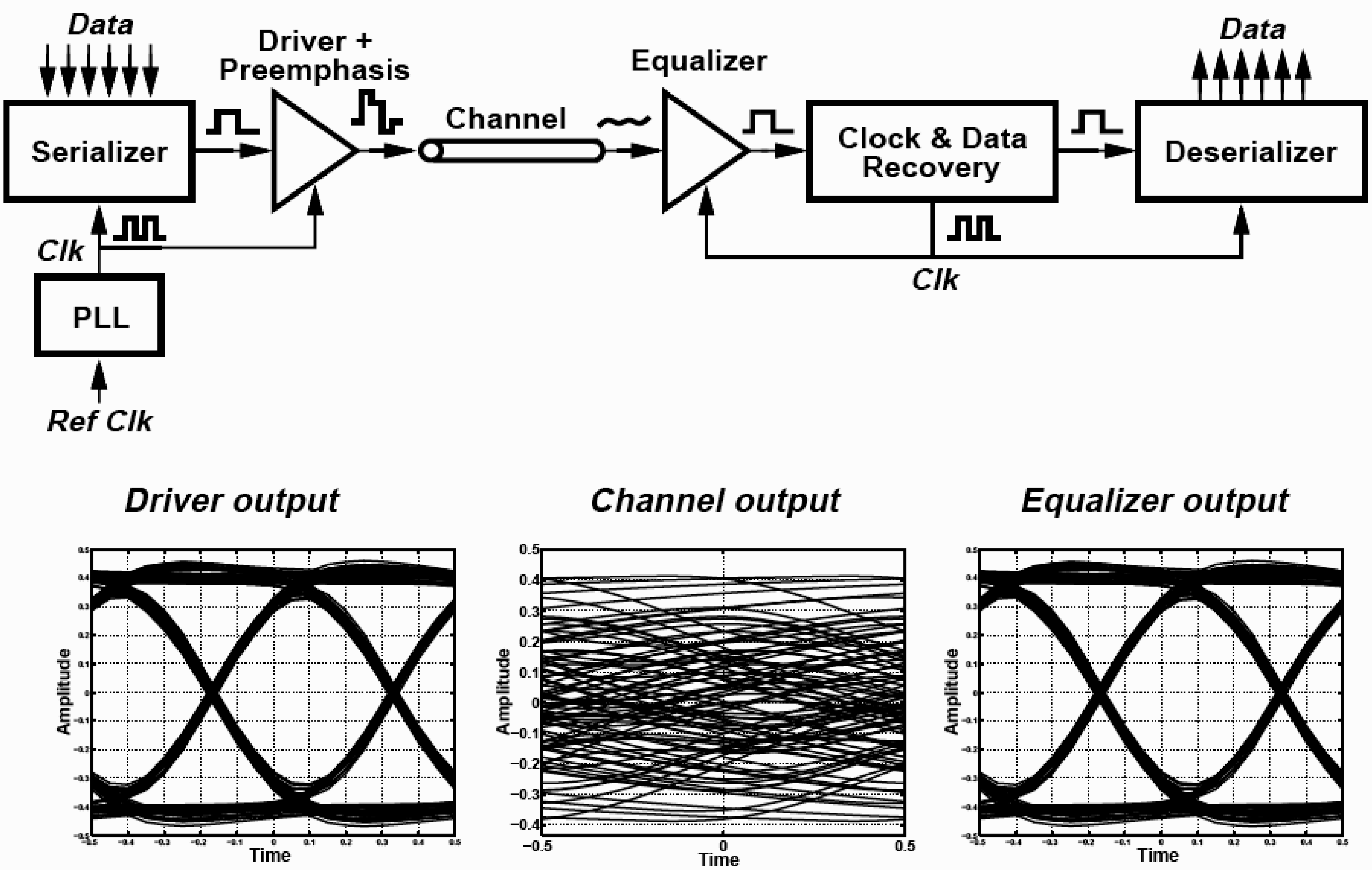


Today's applications require data to be transmitted in Gbps range, often in "unfriendly" environment

- Microprocessors and memories on printed-circuit boards (PCBs).
- Backplane environment involving multitude of PCBs.
- Server & Networking equipment transferring data between boards
- Gigabit Ethernet applications

[Courtesy, Srikanth Gondi]

Serial Link Architecture

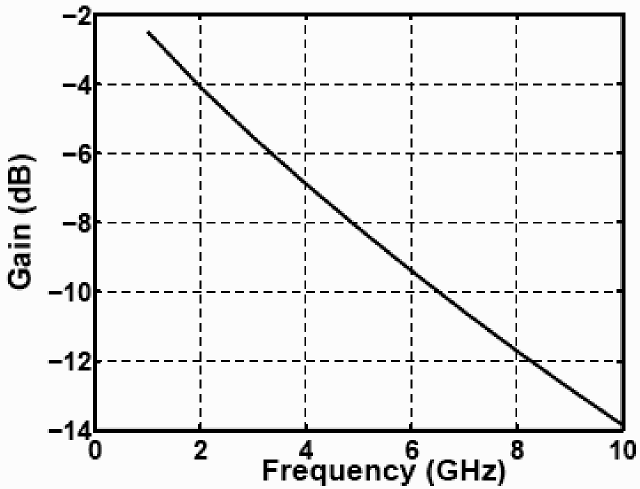


[Courtesy, Srikanth Gondi]

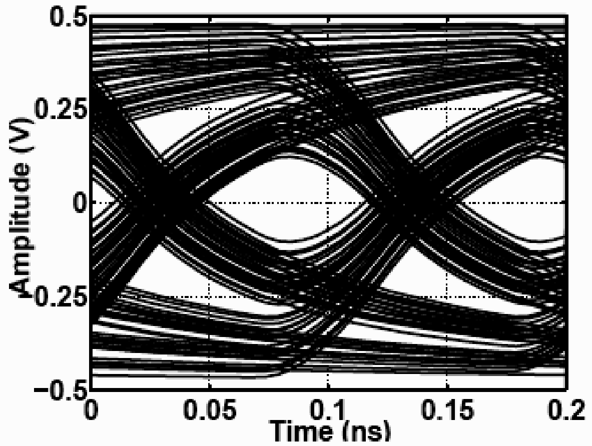
Intersymbol Interference (ISI)

- Frequency-dependent losses in the channel cause ISI
  - ➪ Increased jitter makes clock recovery difficult
  - ➪ Reduced symbol amplitudes lead to higher bit error rate (BER)

12-in FR4 Frequency Response



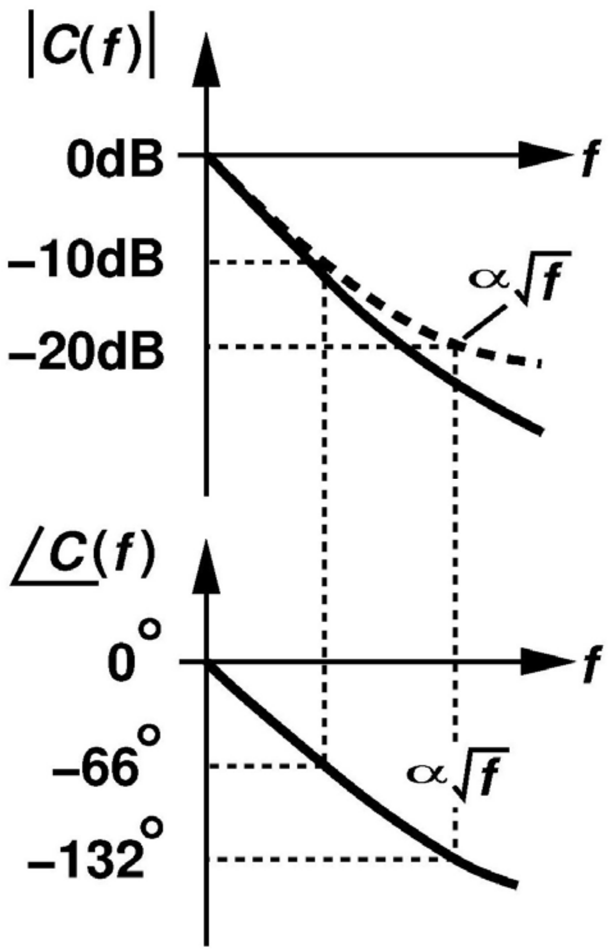
Output Signal at 10 Gb/s



- Eye closure proportional to loss
  - Eye is half closed for 5 dB of loss at 5 GHz
  - Eye is fully closed for 10 dB of loss at 5 GHz

[Courtesy, Srikanth Gondi]

Universal Expression of Wire Loss



$$C(f)=\exp[-k_s l(1+j)\sqrt{f}-k_d l f]$$

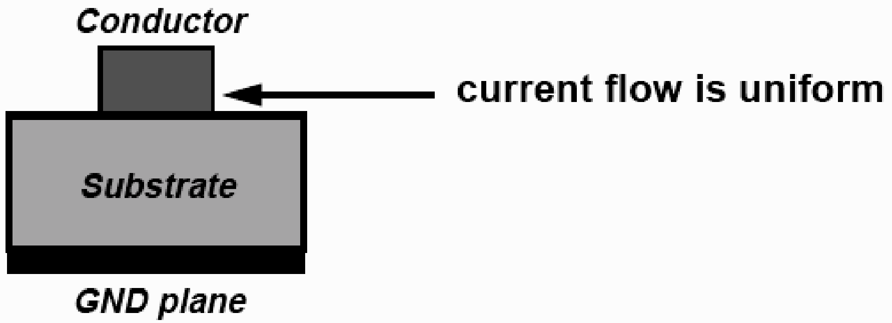
Skin Effect: $-k_s l(1+j)\sqrt{f}$ Dielectric Loss: $-k_d l f$

- Coefficients k_s and k_d vary significantly for different media.
- For example, backplane traces suffer from skin effect more seriously.

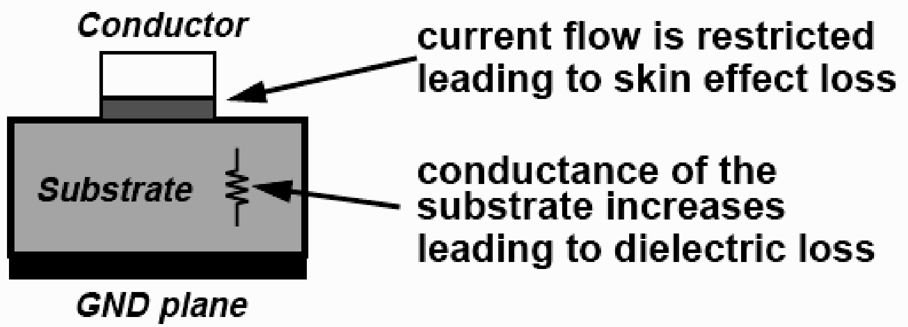
Loss Mechanisms in Microstrips

Microstrip

At low frequencies,



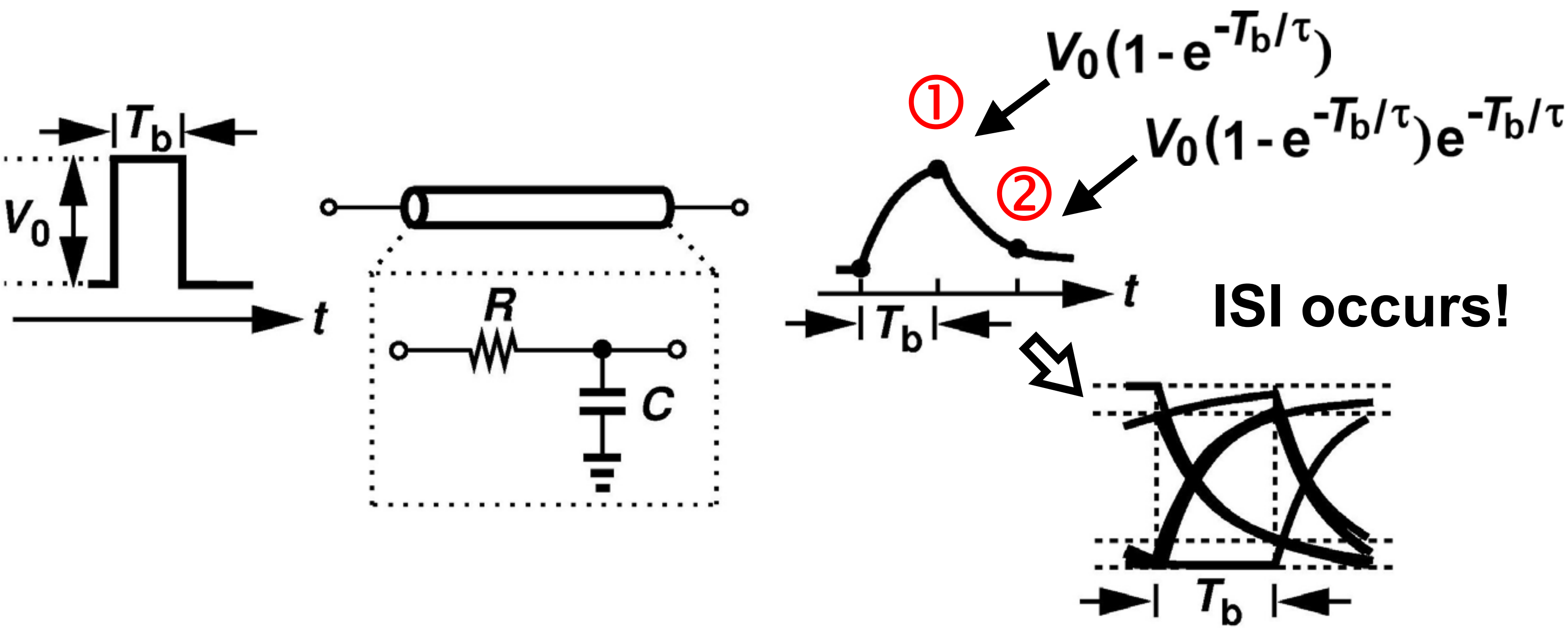
At high frequencies,



- Skin effect loss (in dB) $\propto \sqrt{f}$
- Dielectric loss (in dB) $\propto f$
- Dielectric loss is more pronounced at high frequencies (Beyond 2 GHz, dielectric loss > skin effect loss)

[Courtesy, Srikanth Gondi]

Time-Domain Analysis of Pre-Emphasis

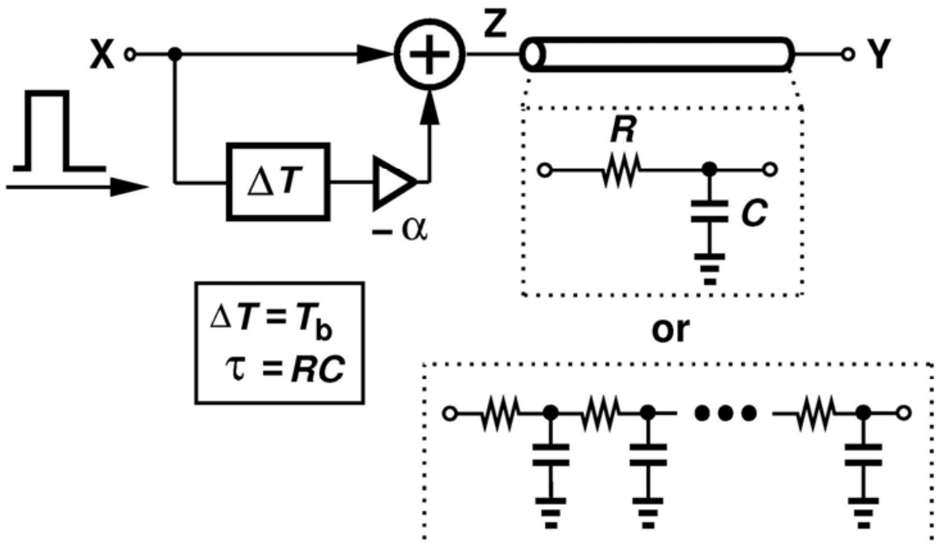


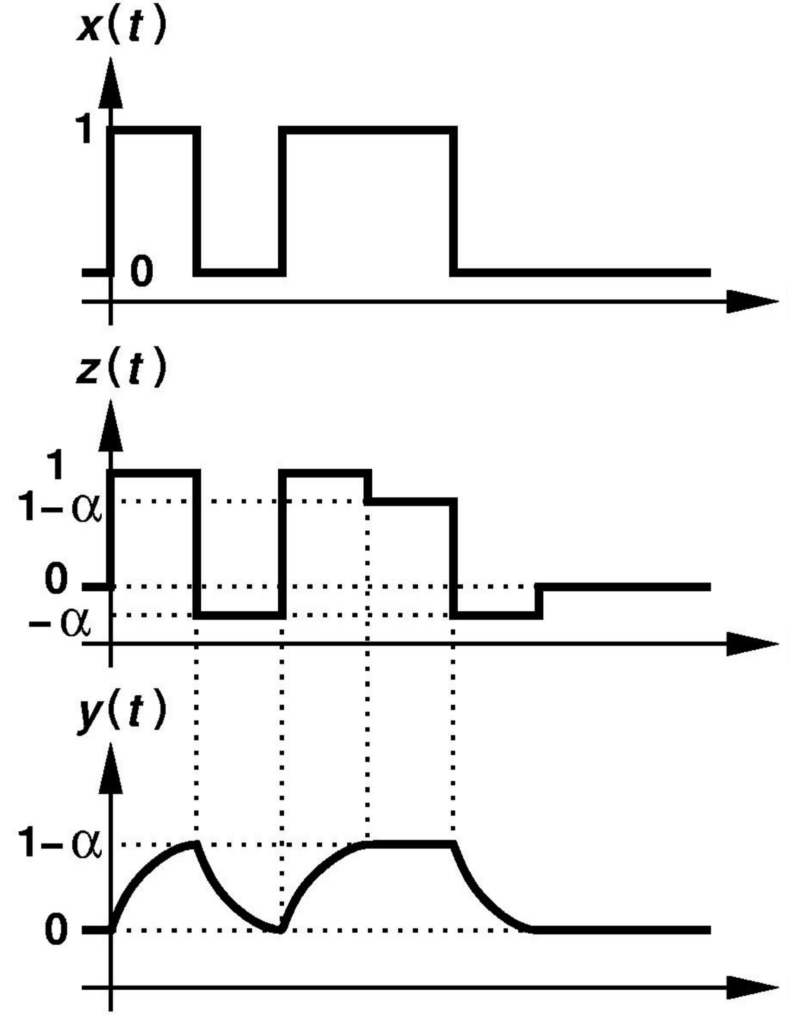
ISI occurs!

- **Insufficient bandwidth leads to ISI.**
- **What happen if we force point ② to zero?**

Time-Domain Analysis of Pre-Emphasis

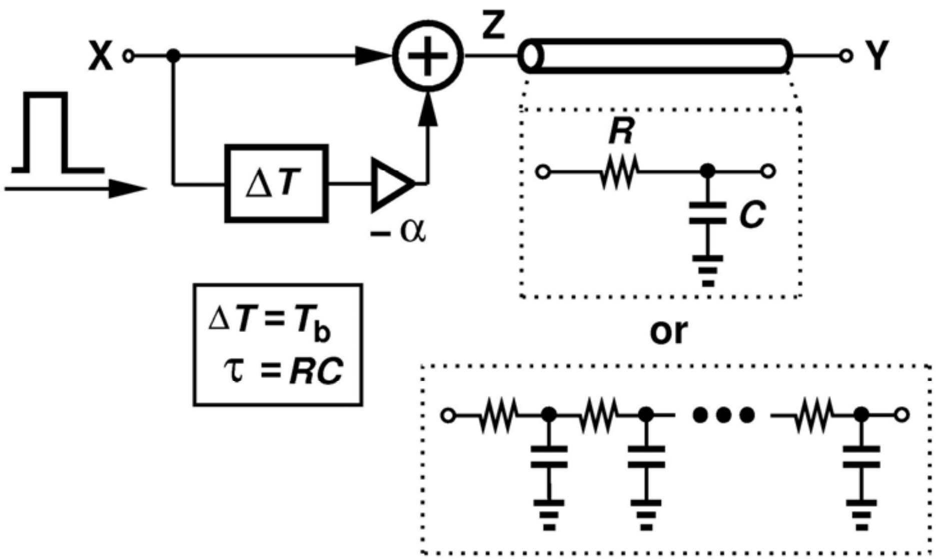
- Two-Tap FIR Filter

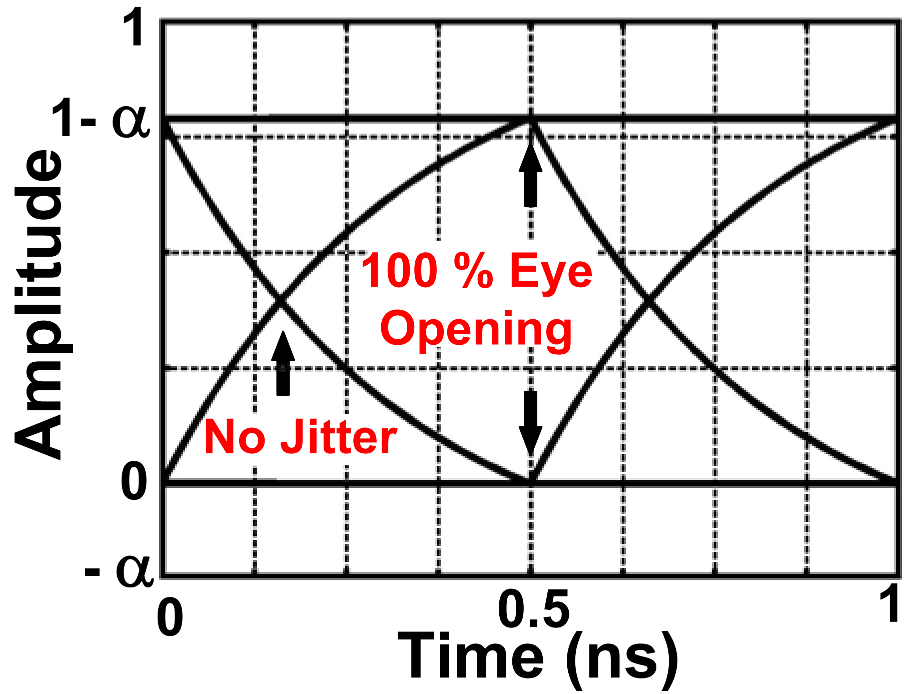




- ISI gets reduced by boosting transition bits.

Time-Domain Analysis of Pre-Emphasis

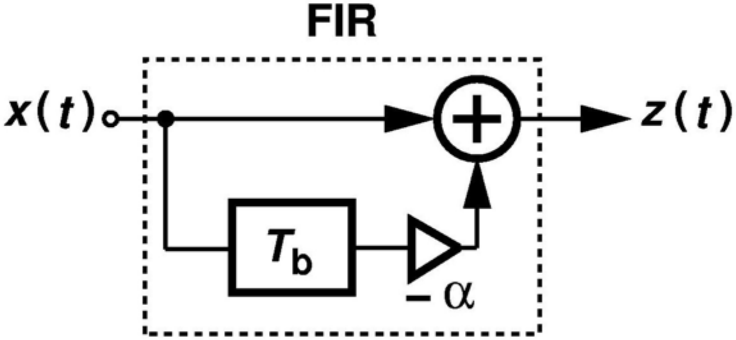


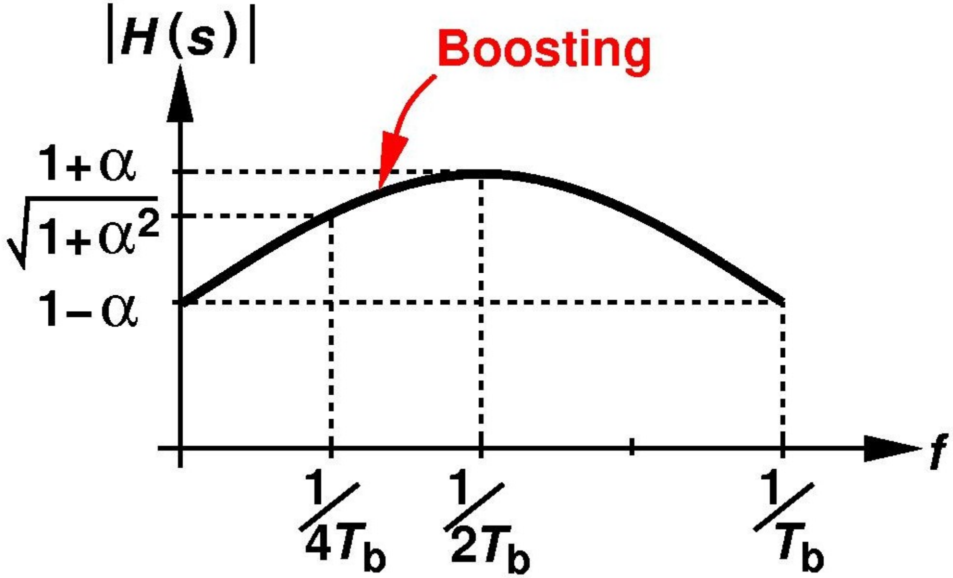


- For any arbitrary τ, we choose $\alpha = \exp(-T_b/\tau)$

➡ **Complete eye opening and zero transition jitter!**
(Of course, it is too good to be true!!)

Frequency Response of Two-Tap FIR





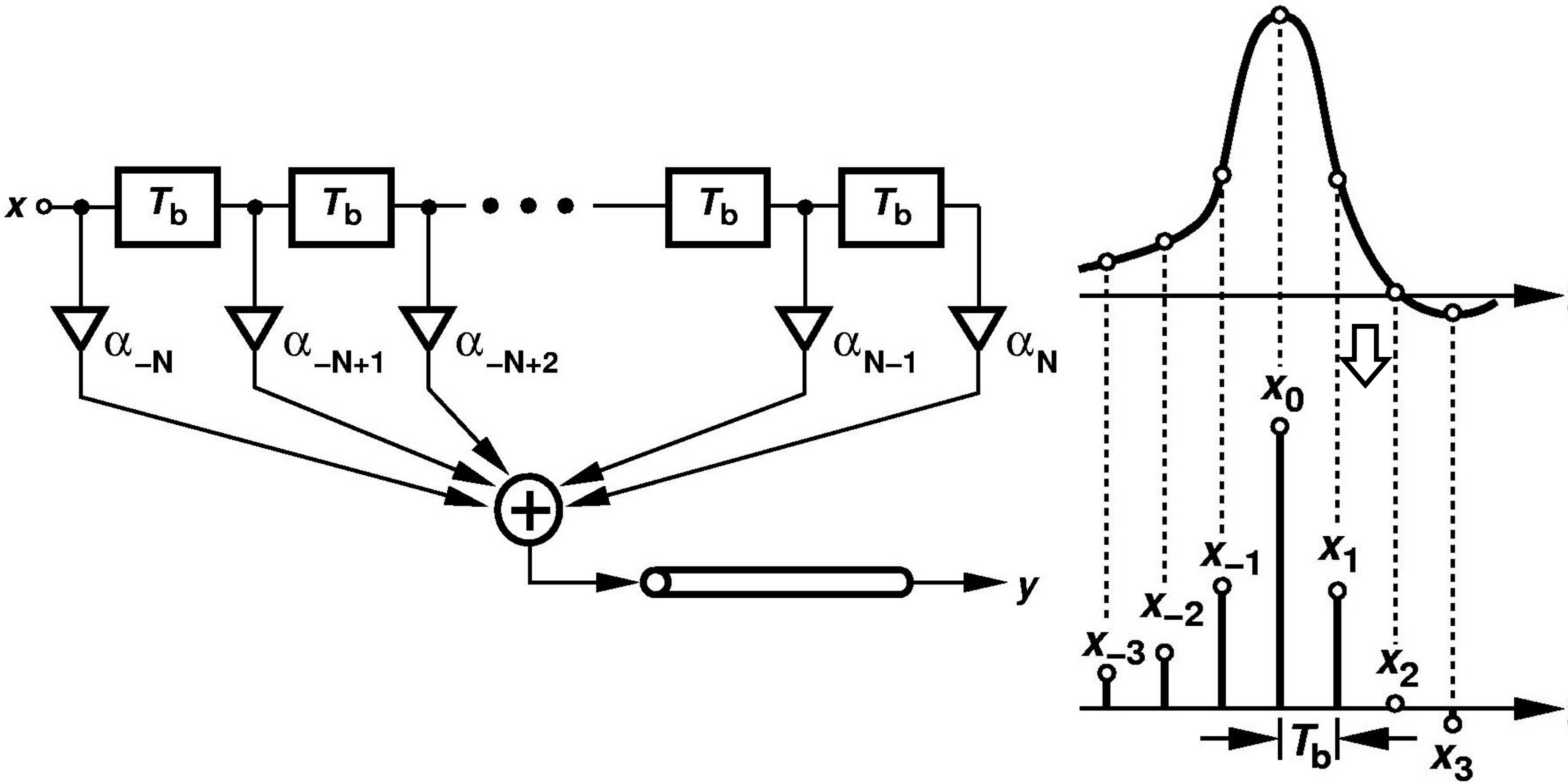
$$z(t) = x(t) - \alpha x(t - T_b)$$

$$H(s) = 1 - \alpha e^{-sT_b}$$

$$Z(s) = X(s)\left[1 - \alpha e^{-sT_b}\right]$$

$$|H(s)| = \sqrt{1 + \alpha^2 - 2\alpha\cos\omega T_b}$$

Multi-Tap FIR Filter with Zero-Forcing



- Impulse response reveals what appears in the output.
- Since the actual waveform is a linear combination of all taps, properly selecting coefficients can eliminate ISI.

Zero-Forcing Technique

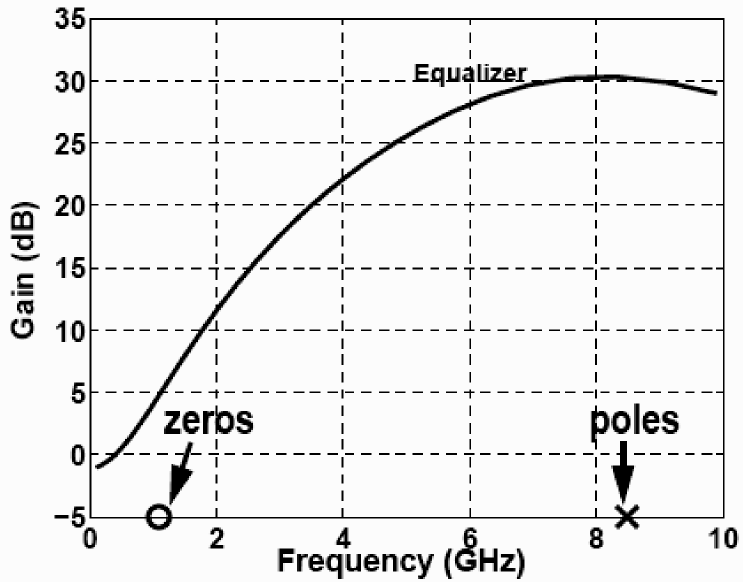
- Since $y_k = \sum_{n=-N}^{N} a_n x_{k-n} = \begin{cases} 1 & \text{for } k = 0 \\ 0 & \text{elsewhere} \end{cases}$, we have

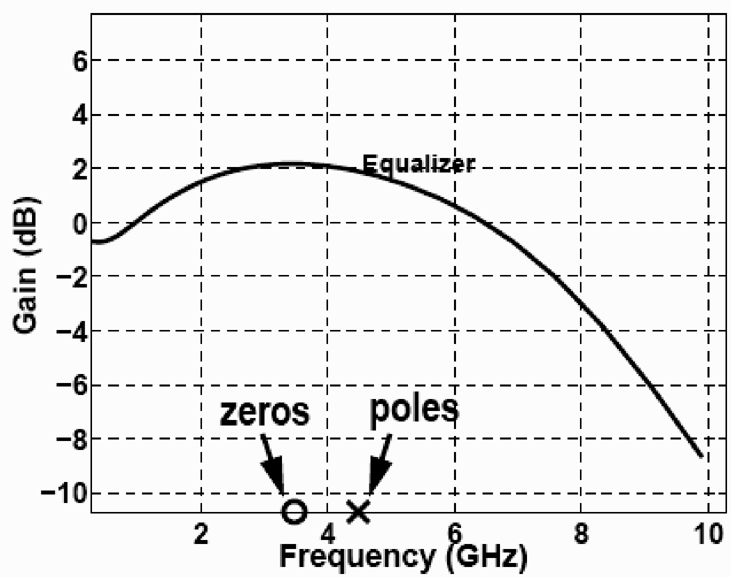
$$\begin{bmatrix} x_0 & x_{-1} & \cdots & x_{-N} & \cdots & x_{-2N-1} & x_{-2N} \\ x_1 & x_0 & \cdots & x_{-N+1} & \cdots & x_{-2N} & x_{-2N+1} \\ \vdots & \vdots & & & & & \\ x_N & x_{N-1} & \cdots & x_0 & \cdots & x_{-N-1} & x_{-N} \\ \vdots & \vdots & & & & & \\ x_{2N-1} & x_{2N-2} & \cdots & x_{N-1} & \cdots & x_{-2} & x_{-1} \\ x_{2N} & x_{2N-1} & \cdots & x_N & \cdots & x_{-1} & x_0 \end{bmatrix} \begin{bmatrix} a_{-N} \\ a_{-N+1} \\ \vdots \\ a_0 \\ \vdots \\ a_{N-1} \\ a_N \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 1 \\ \vdots \\ 0 \\ 0 \end{bmatrix}$$

- Zero ISI requires infinite length.
- Zero forcing only occurs at sampling points (discrete behavior), issues such as transition jitter are not considered here.

Equalizer Filter Design

- Basic strategy is to place "zeros" at low frequencies and "poles" at high frequencies.
- Equalizer filters can be realized with
  - Real zeros and real poles
  - Real zeros and complex poles (low Q)
  - Complex zeros and complex poles (low Q)
- Tunability

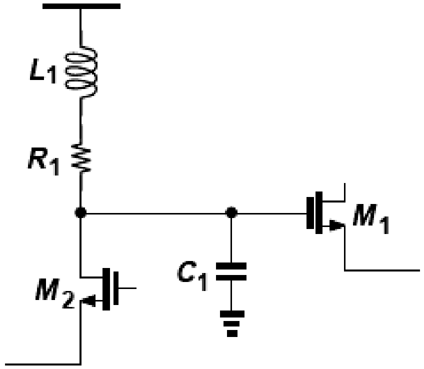


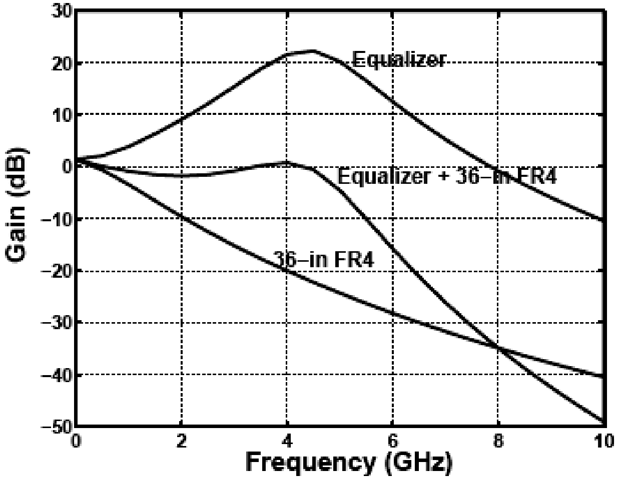


[Courtesy, Srikanth Gondi]

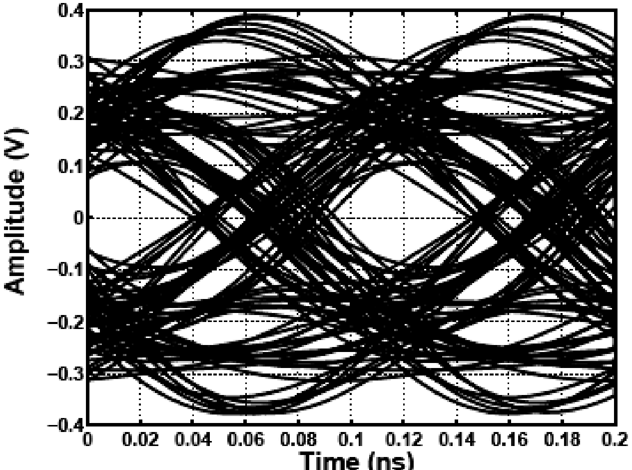
Second Order Structures

$$T(s) = \frac{k(s+z)}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2}$$





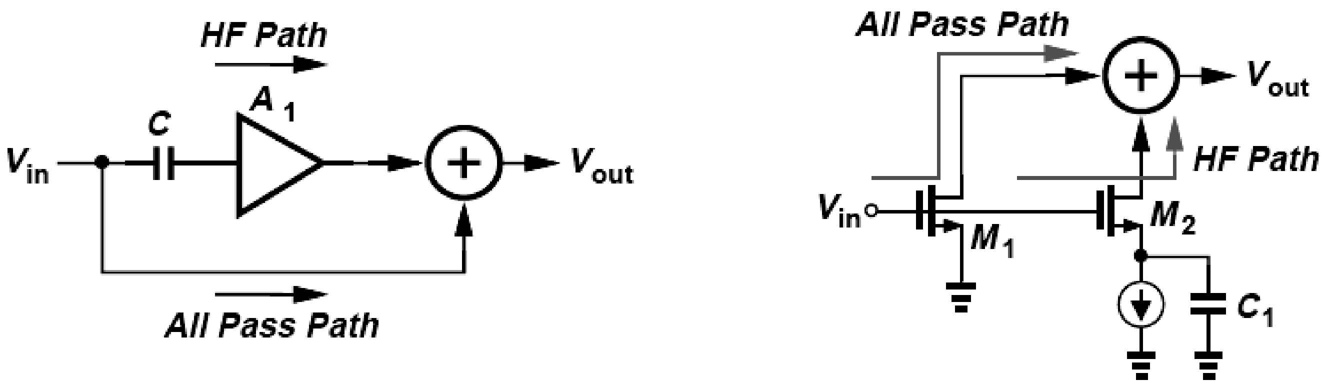
- Second order structures reasonably match the inverse of FR4
- Issues
  - Jitter response is bad due to phase response
  - Atmost 6 dB of high frequency boost at the cost of two poles

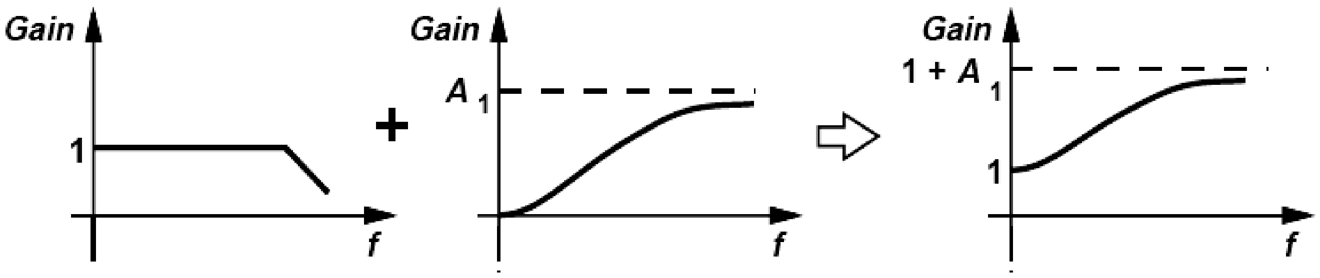


[Courtesy, Srikanth Gondi]

Equalizer Filter: Intuitive Approach

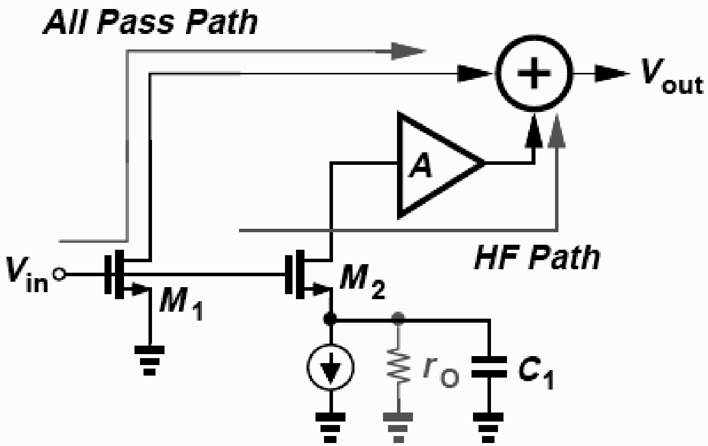
Illustration of the parallel path approach

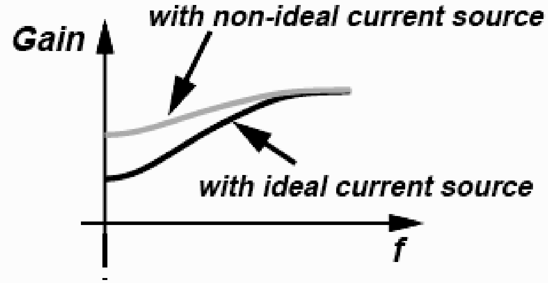




[Courtesy, Srikanth Gondi]

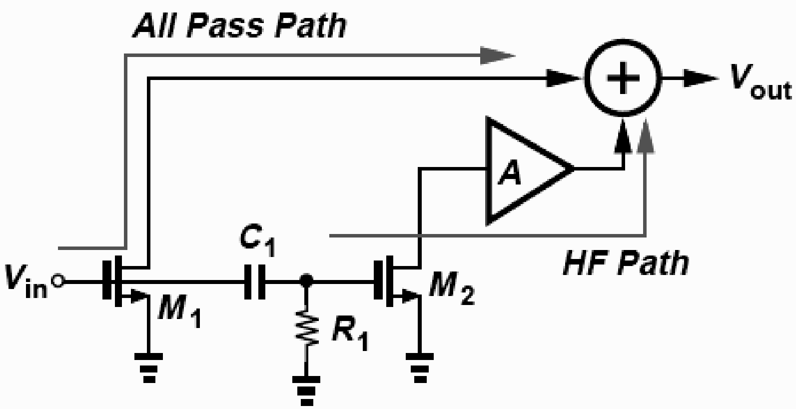
Parallel Path Approach





- Finite r_o makes this approach very inefficient
- Is a good bandwidth extension technique

Alternative approach

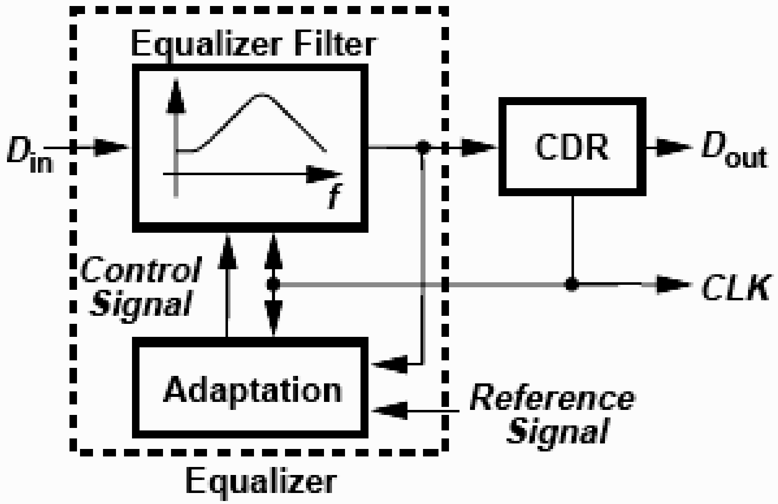


- Each stage BW is 6GHz, ➪ two stage BW < 4GHz
- Satisfies all requirements except bandwidth and linearity

[Courtesy, Srikanth Gondi]

Review of Prior Art

Tomita, IEEE VLSI Symposium, Jun. 2004.
Stojanovic, IEEE VLSI Symposium, Jun. 2004.
Balamurugan, IEEE VLSI Symposium, Jun. 2004.
Farjad-Rad, IEEE VLSI Symposium, Jun. 2003.
Choi, IEEE VLSI Symposium, Jun. 2003.
Zerbe, IEEE JSSC, Dec. 2003.
Green, IEEE ISSCC, Feb. 2003.

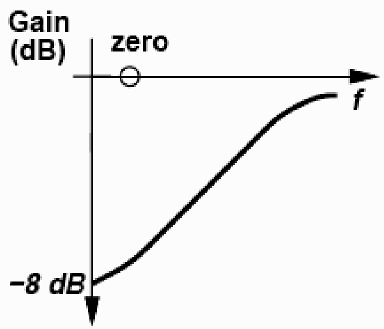


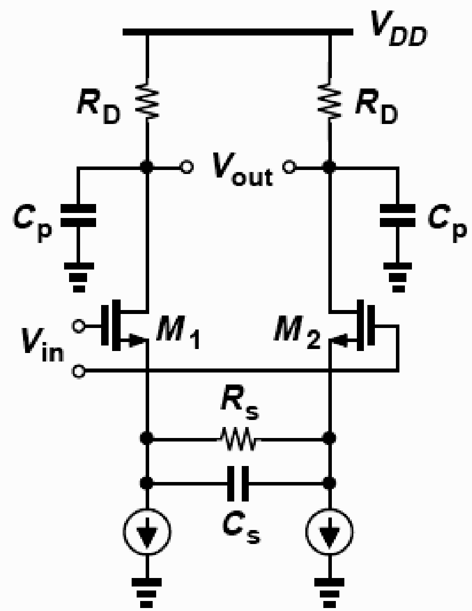
- One or more of the following issues persist with existing designs
  - Speed Limitations
  - Large Power Dissipation
  - Large Jitter
  - Lack of Adaptibility
  - Limited Trace Length
  - Realized in Bipolar process

[Courtesy, Srikanth Gondi]

RC Source Degeneration

$$\frac{V_{out}}{V_{in}} = \frac{g_m R_D (1 + R_s C_s s)}{\left(1 + \frac{g_m R_s}{2} + R_s C_s s\right)(1 + R_D C_p s)}$$





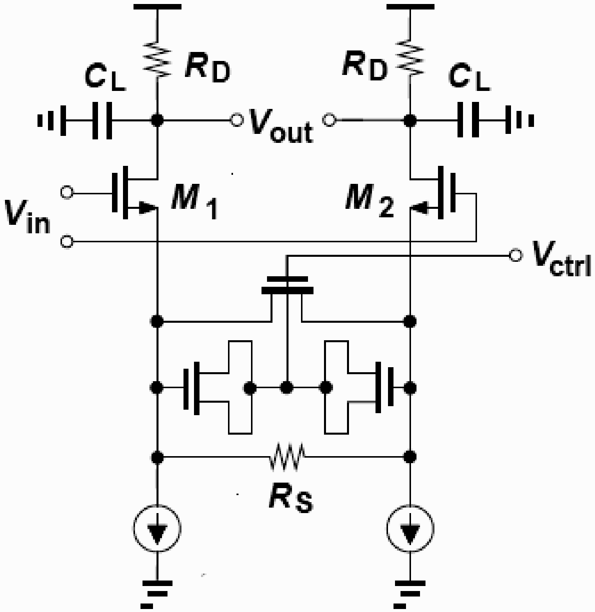
- Source degeneration structure is a good candidate as a filter :
  - High frequency boost of 8 -10dB with 10 GHz bandwidth
  - Good linearity
- Limitation is high DC loss

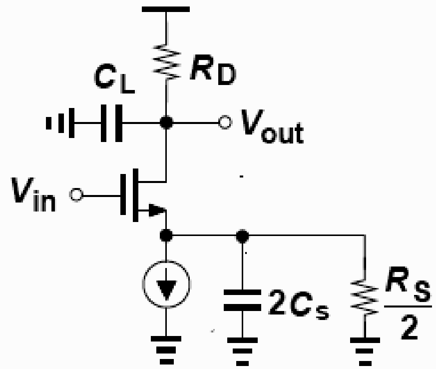
➪ With 5 stages overall, bandwidth < 3.8GHz

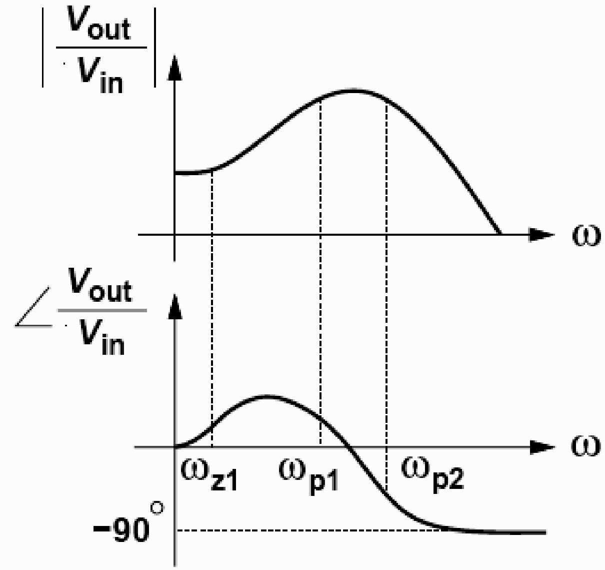
➪ Require a new technique to improve bandwidth

[Courtesy, Srikanth Gondi]

Conventional Filter Stage







$$\frac{V_{out}}{V_{in}}(s) = \frac{g_{m1}R_D}{1+\frac{g_{m1}R_S}{2}} \cdot \frac{1+\frac{s}{\omega_{z1}}}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$$

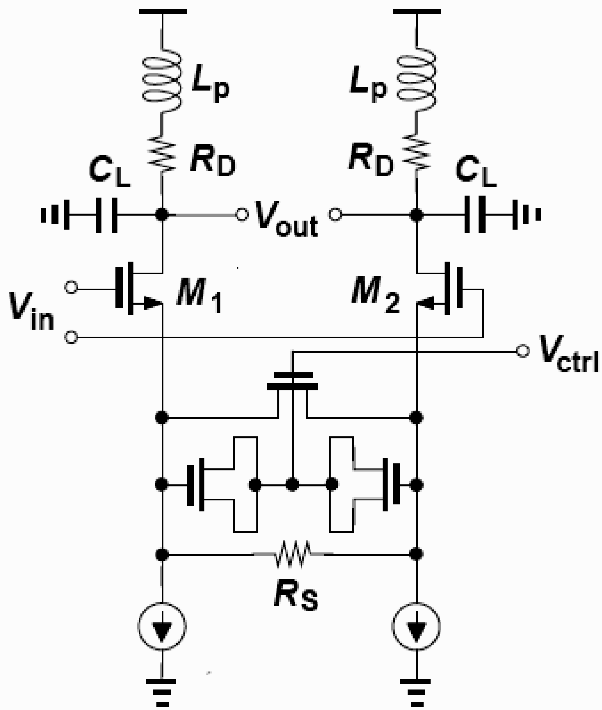
$$\omega_{z1} = \frac{1}{R_S C_S}$$

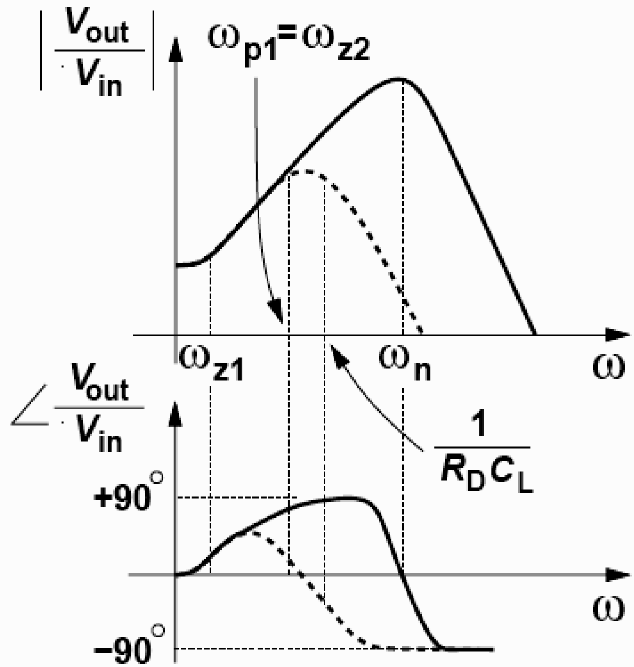
$$\omega_{p1} = \frac{1+g_{m1}R_S/2}{R_S C_S}$$

$$\omega_{p2} = \frac{1}{R_D C_L}$$

⇨ **Severe tradeoff between gain and boosting.**

Filter Stage with Inductive Peaking





$$\omega_{z1} = \frac{1}{R_S C_S}$$

$$\omega_{p1} = \frac{1 + g_{m1} R_S / 2}{R_S C_S}$$

$$\omega_{z2} = 2\zeta\omega_n$$

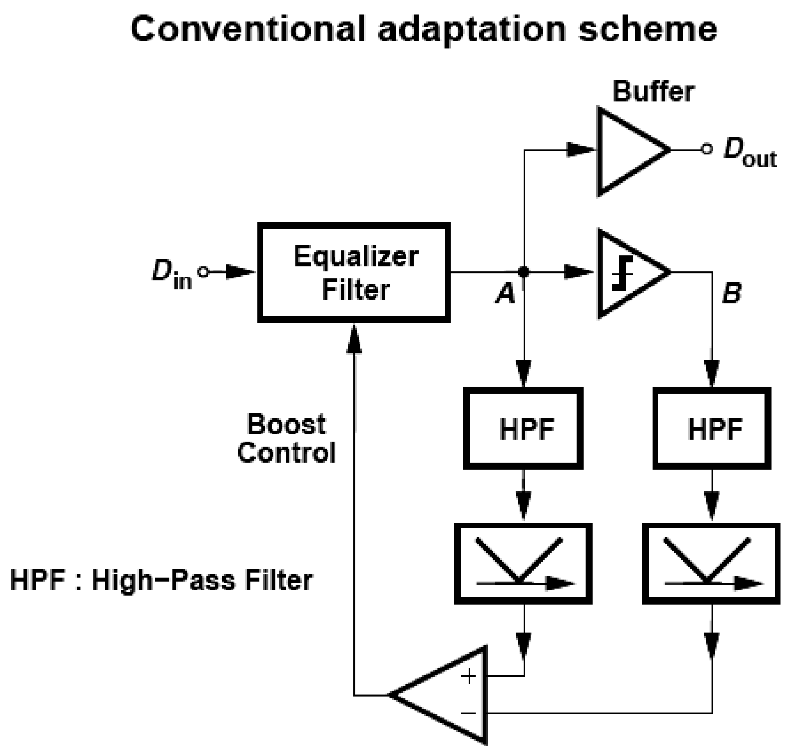
$$\zeta = \frac{1}{R_S C_S}$$

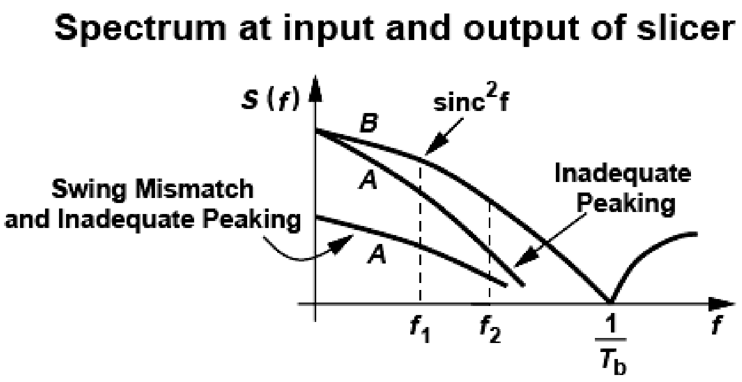
$$\omega_n = \frac{1}{\sqrt{L_P C_L}}$$

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_{m1} R_D}{1 + \frac{g_{m1} R_S}{2}} \cdot \frac{1 + \frac{s}{\omega_{z1}}}{1 + \frac{s}{\omega_{p1}}} \cdot \frac{1 + \frac{s}{\omega_{z2}}}{1 + \frac{2\zeta}{\omega_n} s + \frac{s^2}{\omega_n^2}}$$

- The second zero extends the gain boosting and phase compensation by canceling the first pole.

Problem of Adaptation

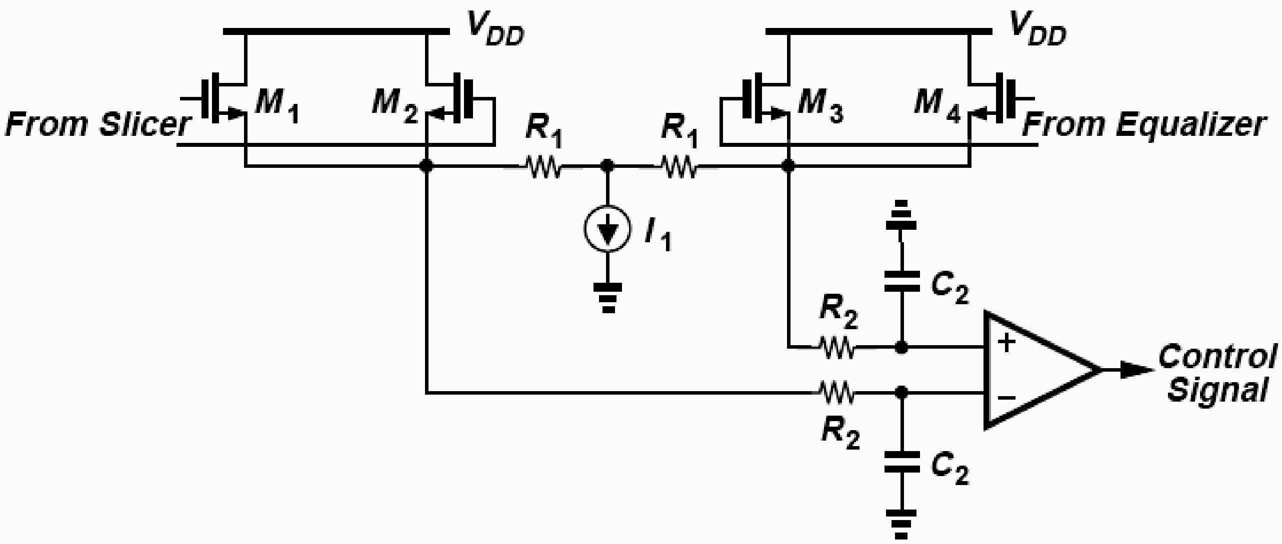


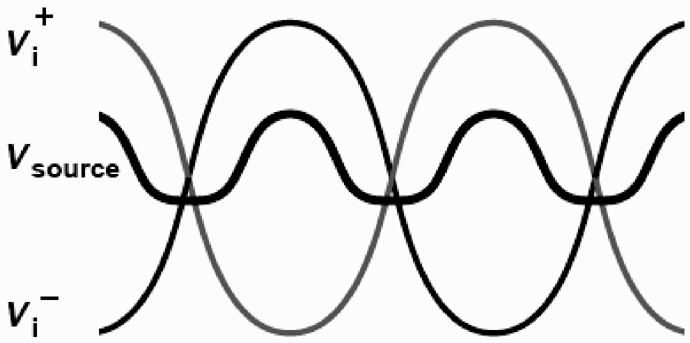


[Courtesy, Srikanth Gondi]

Rectifier & Integrator

Rectifier and Error Amplifier

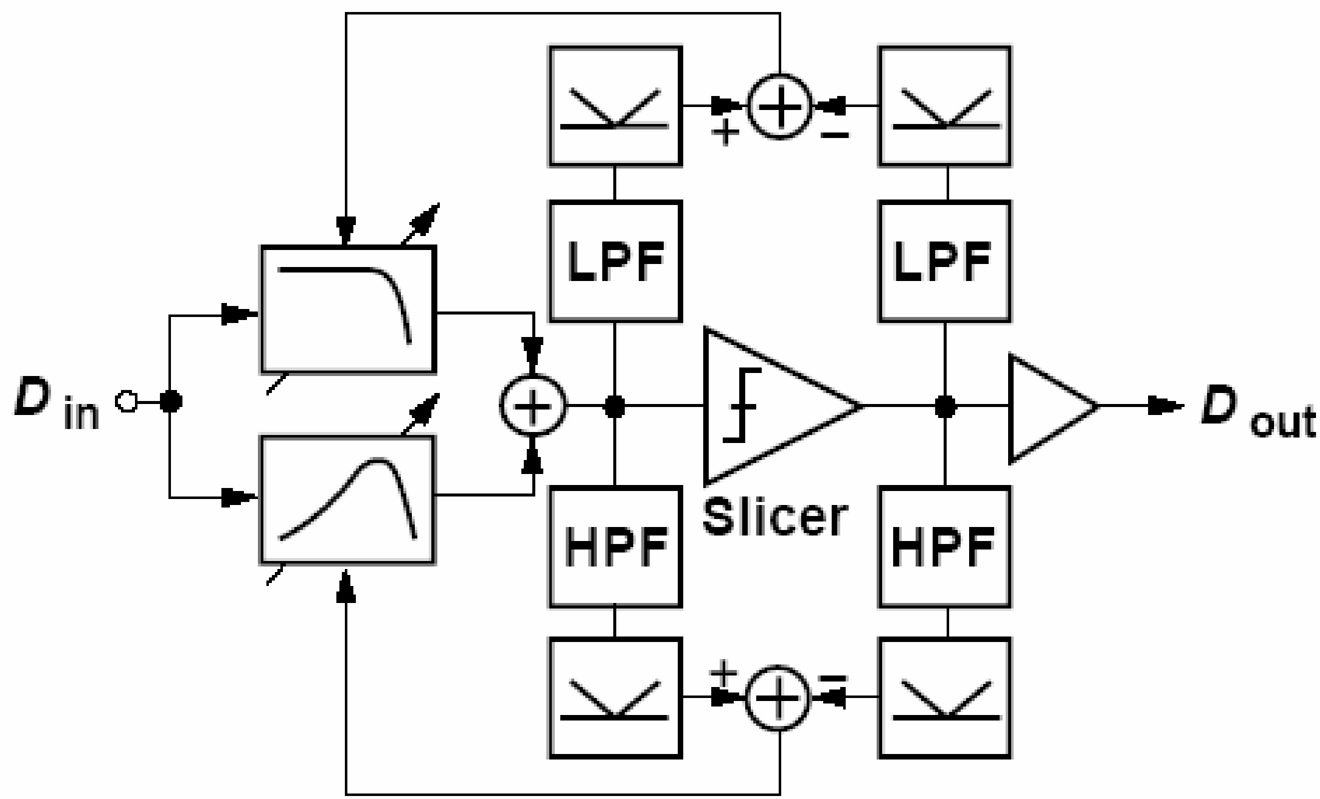




Rectifier response

[Courtesy, Srikanth Gondi]

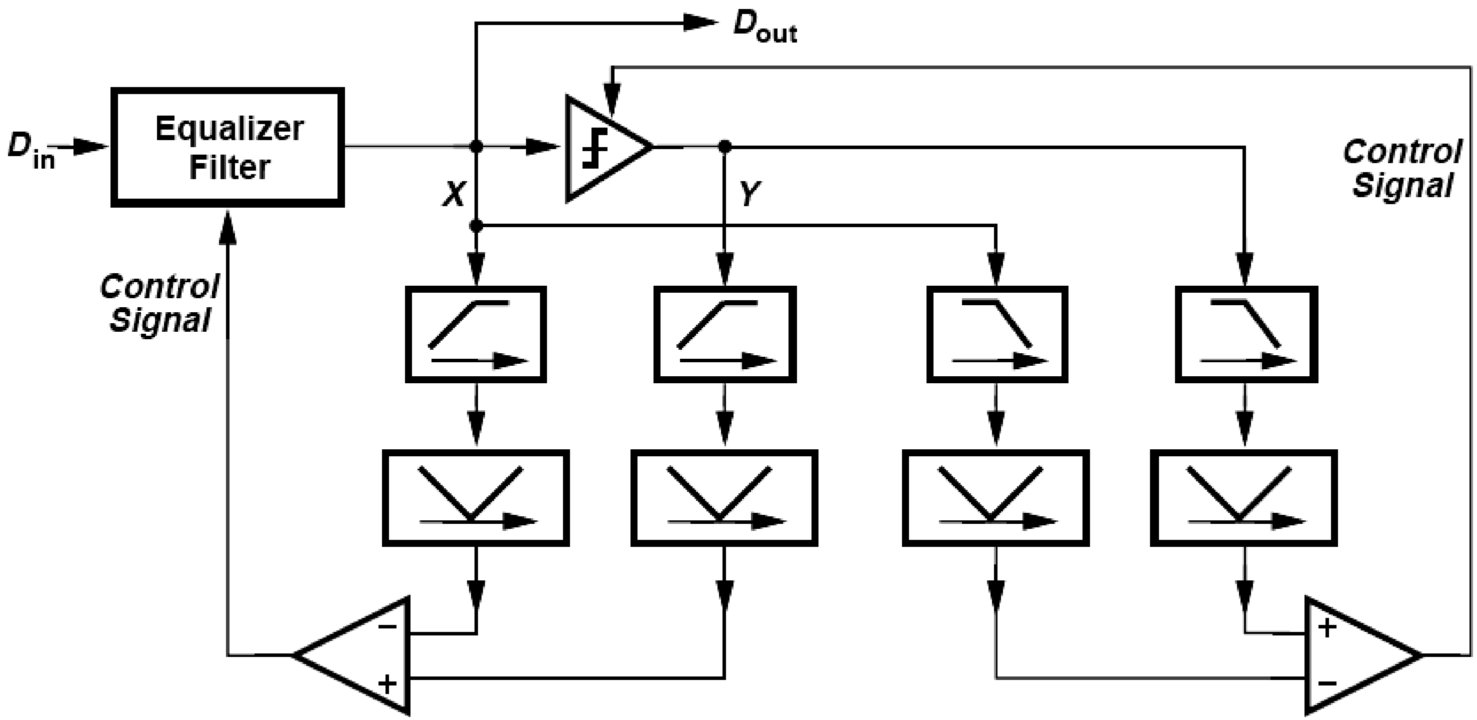
Case Study I



[Choi, 04]

- Dual loop architecture to balance low- and high-frequency parts.

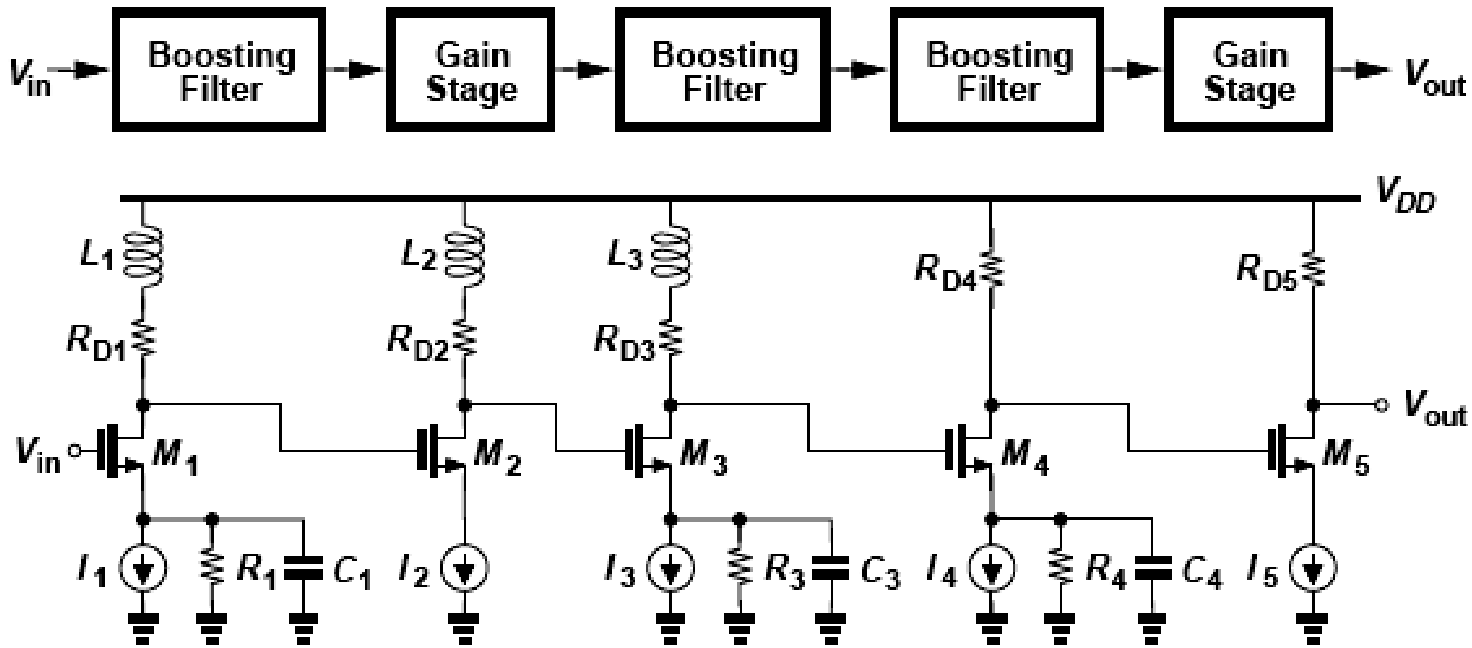
Case Study II



- Two feedback loops
  - High-frequency boost control in the equalizer filter
  - DC level control in the comparator

[Gondi, 05]

Case Study II



Stage j	W_j (μm)	I_j (mA)	R_j ($k\Omega$)	C_j (fF)	$R_{D,j}$ ($k\Omega$)	L_j (nH)
1	36	2	0.5	260	0.18	0.8
2	22	1.8	–	–	0.18	3
3	16	0.9	0.5	170	0.43	3.5
4	14	0.5	0.55	130	0.75	–
5	6	0.3	–	–	1.25	–

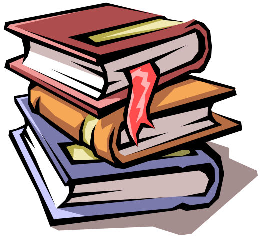
- Actual design is differential

[Gondi, 05]

Oscillators (I)

Professor Jri Lee

台大電子所　李致毅教授

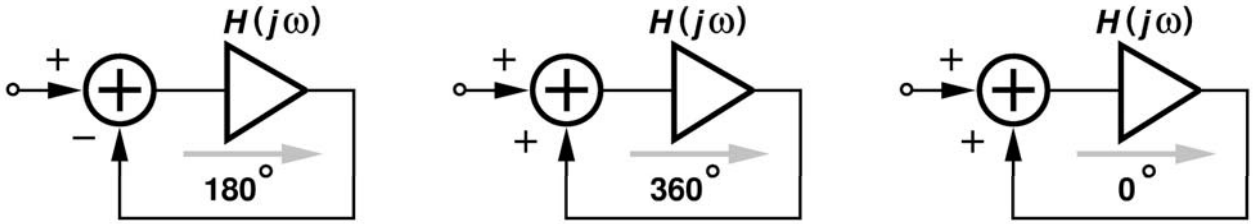


Electrical Engineering Department
National Taiwan University

Outline

- Barkhausen Criteria
- Ring Oscillators
- LC Oscillators
- Colpitts Oscillator
- Tuning Techniques

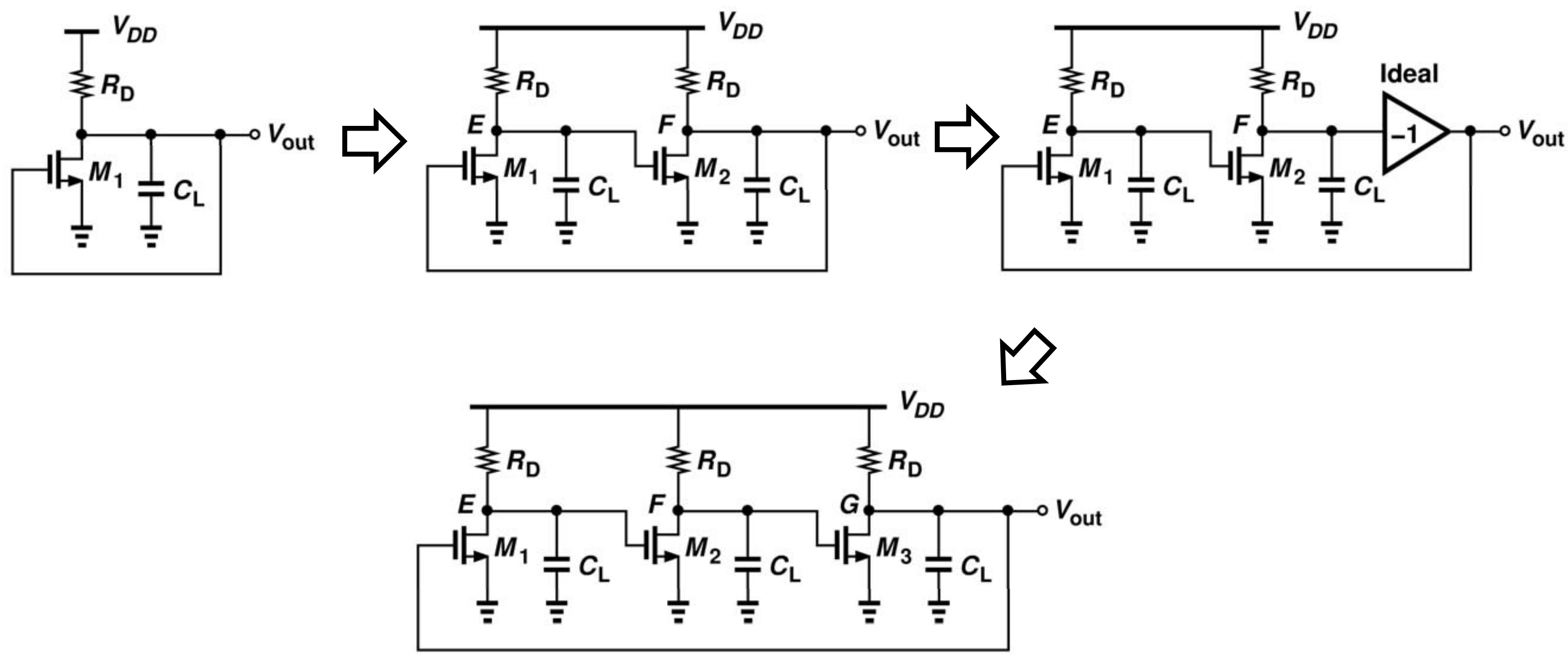
BarkhausenCriteria



$$\left|H(j\omega_0)\right| \geq 1, \quad \angle H(j\omega_0) = 180^\circ$$

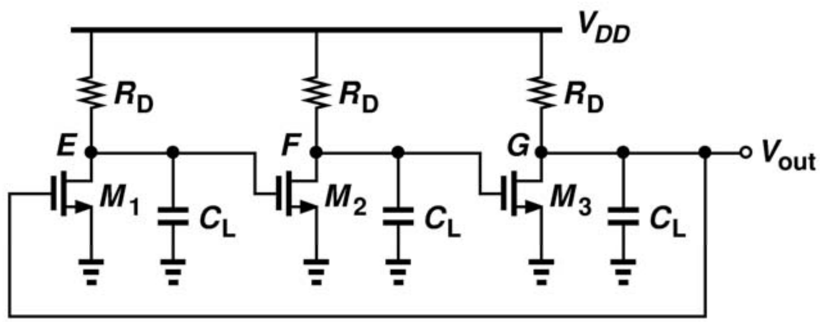
- Poles locate at the y-axis.
- Necessary but not sufficient.
- Loop gains are typically chosen to be at least 2 or 3 to ensure oscillation. Oscillators adjust themselves to satisfy the criteria.

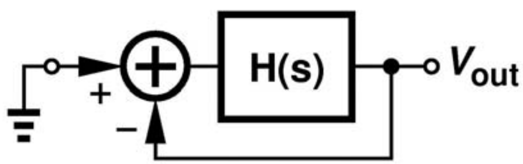
Evolution of Ring Oscillators



- Barkhausen criteria is achievable only when the number of stage is greater than 2.

Three-Stage Ring Oscillator





$$H(s) = \frac{A_0^3}{(1 + s/\omega_0)^3}$$

$$A_0 = g_m R_D, \quad \omega_0 = 1/R_D C_L$$

$$\Rightarrow \quad \tan^{-1}(\omega_{osc}/\omega_0) = 60^\circ$$

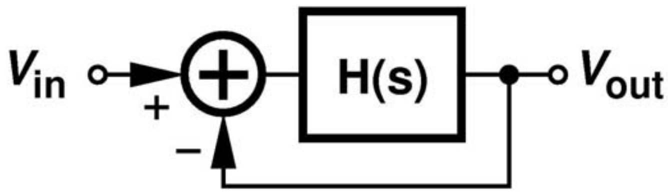
$$\omega_{osc} = \sqrt{3}\omega_0$$

$$\Rightarrow \quad \frac{A_0}{\sqrt{1 + \omega_{osc}^2/\omega_0^2}} = 1$$

$$A_0 \geq 2$$

❒ **Tuning can be included by adjusting R_D or C_L.**

Three-Stage Ring Oscillator

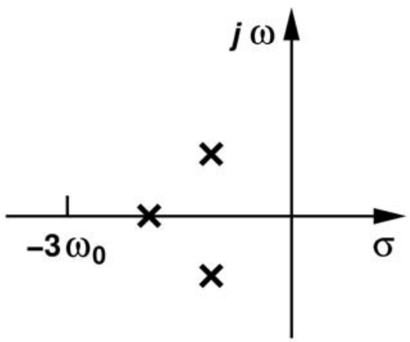


$$\frac{V_{out}}{V_{in}} = \frac{\dfrac{A_0^3}{(1+ s/\omega_0)^3}}{1+\dfrac{A_0^3}{(1+ s/\omega_0)^3}}$$

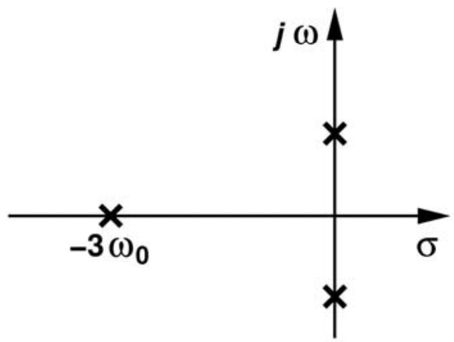
$$H(s) = \frac{V_{out}}{V_{in}}(s) = \frac{A_0^3}{(1+ s/\omega_0)^3}$$

$$s_1 = (-A_0 - 1)\omega_0$$

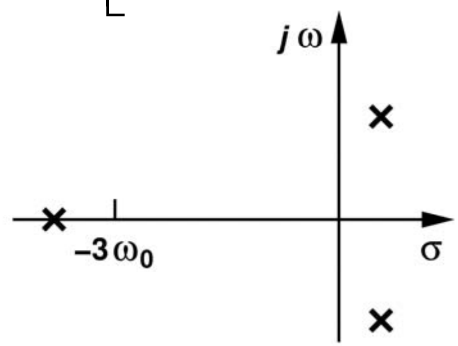
$$s_{2,3} = \left[\frac{A_0(1 \pm j\sqrt{3})}{2} - 1\right]\omega_0$$



$0 < A_0 < 2$



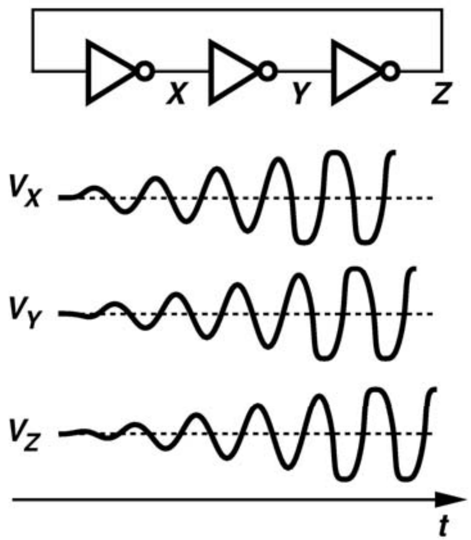
$A_0 = 2$

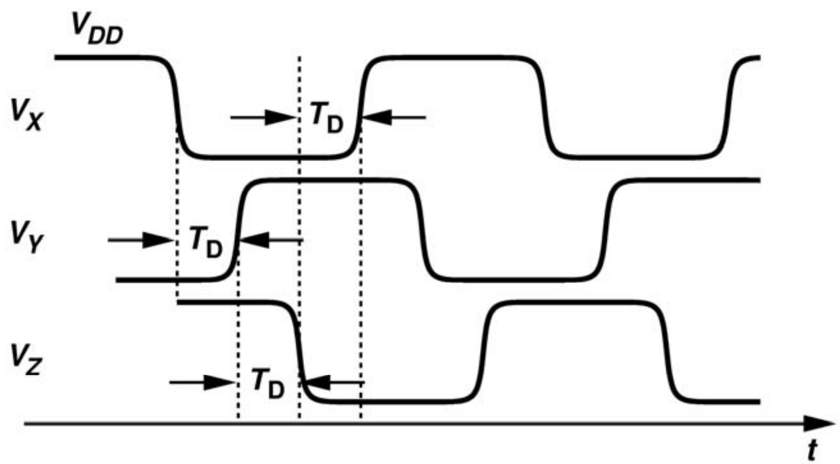


$A_0 > 2$

$$V_{out} \propto \exp\left(\frac{A_0 - 2}{2}\omega_0 t\right)\cos\left(\frac{A_0\sqrt{3}}{2}\omega_0 t\right)$$

Large Signal Analysis

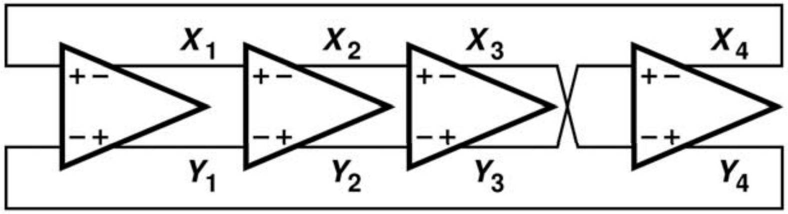




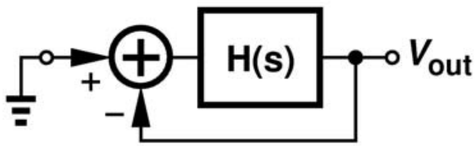
$$\frac{A_0\sqrt{3}\omega_0}{2} \neq 6T_D$$

- In reality, the signal "saturates" to make the average loop gain equal to unity.
- The actual oscillation frequency is determined by large signal behavior.

Four-Stage Ring Oscillators



$$H(s) = \frac{A_0^4}{(1 + s/\omega_0)^4}$$

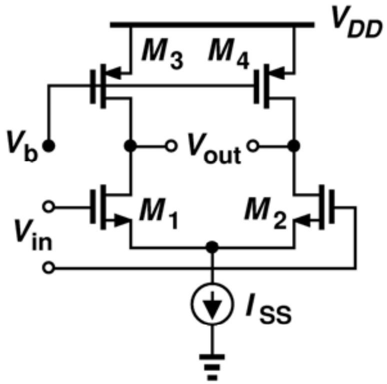


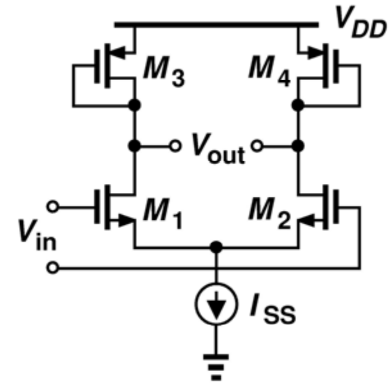
$$\omega_{osc} = \omega_0$$

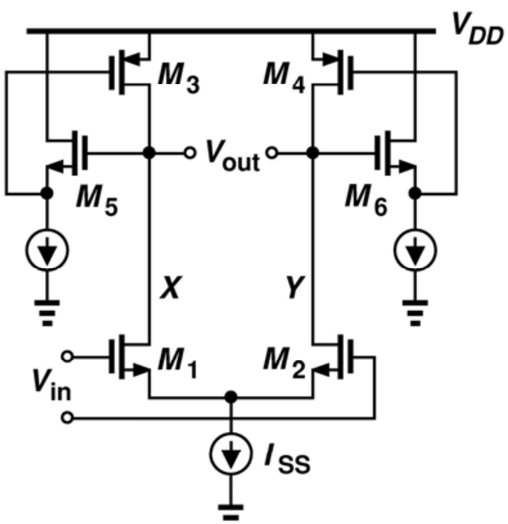
$$A_0 \geq \sqrt{2}$$

- The number of stages in a ring oscillator is determined by speed, power and noise performance.

CMOS Realizations without Resistors





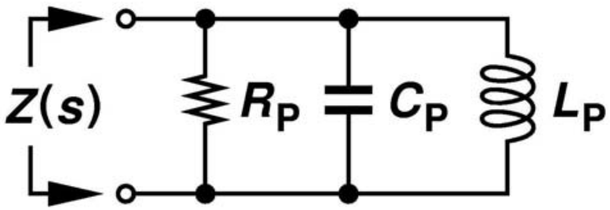


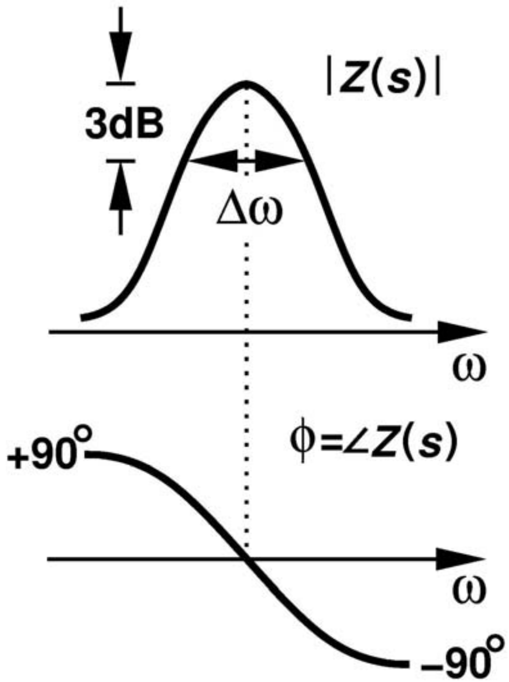
Overcome voltage headroom issue.

- **If poly resistors are available then use them.**

Quality Factor of Inductors

❒ **Definitions**





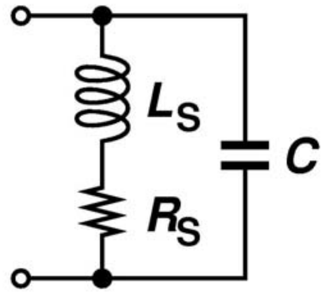
(i) $Q = \frac{\omega_0}{\Delta\omega}$

(ii) $Q = 2\pi \frac{\text{Energy Stored}}{\text{Energy Dissipated Per Cycle}}$

(iii) $Q = \frac{\omega_0}{2} \cdot \frac{d\phi}{d\omega}$

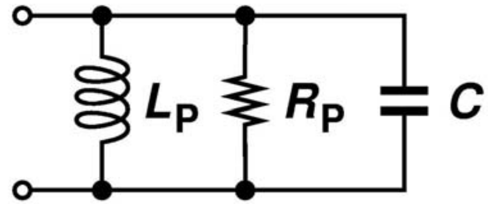
❒ **Three definitions are equivalent.**

Equivalent Circuit of an LC Tank



⇔

$$L_S = L_P$$

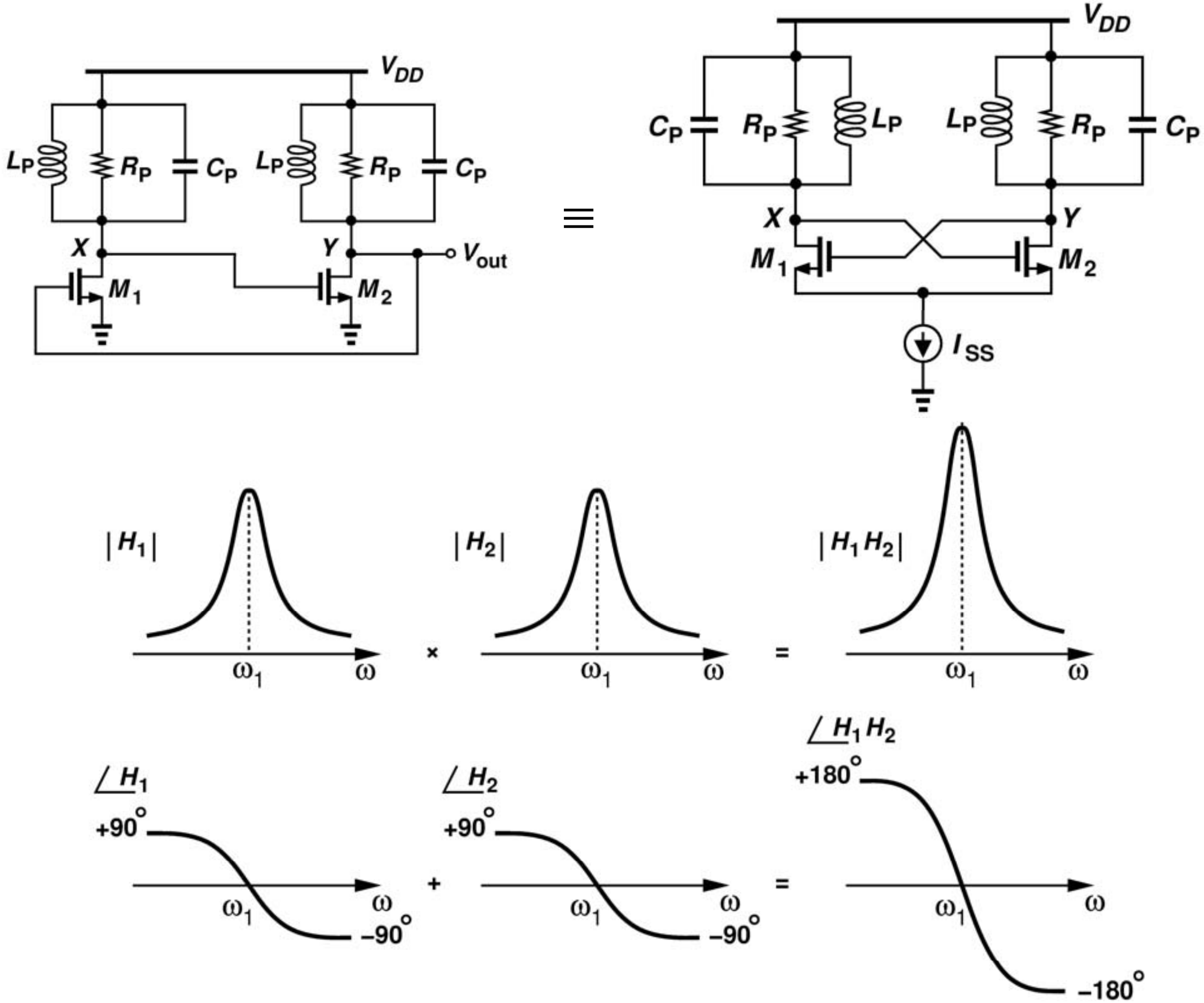


$$R_S = \frac{\omega L_S}{Q}$$

$$R_P = Q \cdot \omega L_P$$

- ❒ *Q* is a function of inductance and frequency.
- ❒ *Q* is around 3-5 for large inductors (>5nH). Smaller inductors typically achieve a higher *Q*.

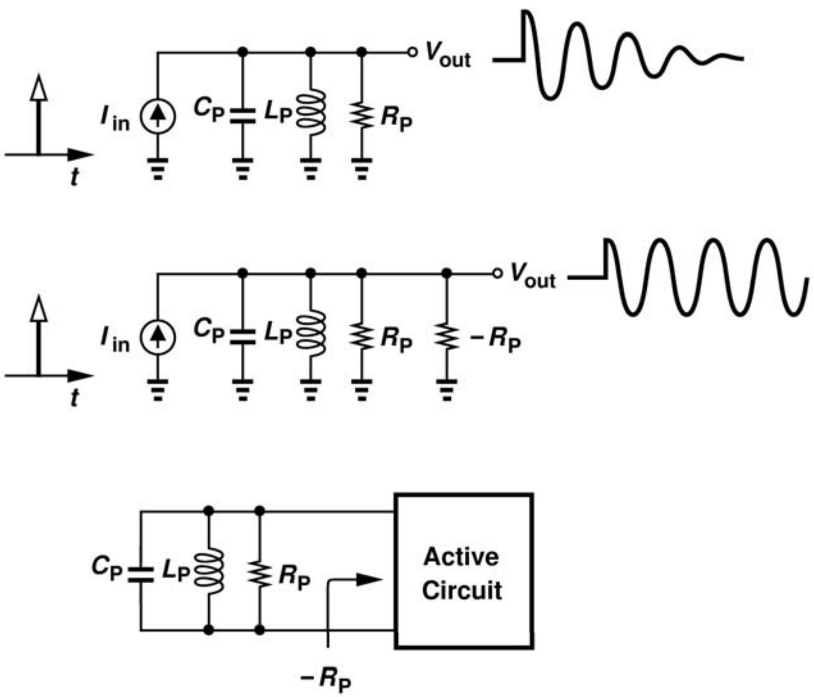
LC Oscillators

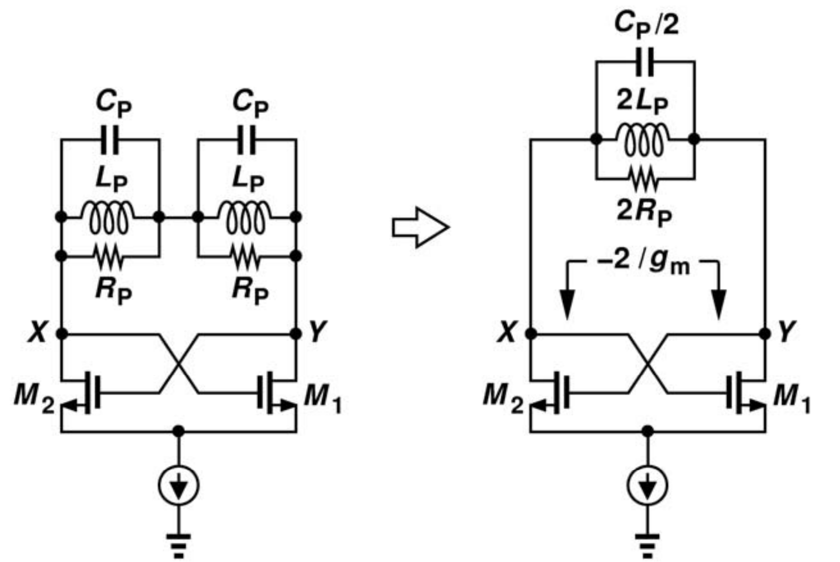


- ❐ **Barkhausen criteria can be easily satisfied.**
- ❐ **Oscillation frequency = ω_1.**
- ❐ **Minimum phase noise point.**

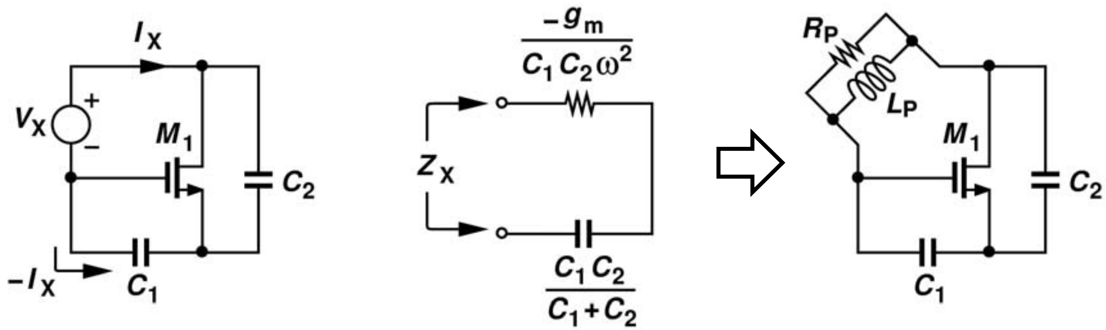
Another Approach to Oscillation

- Cross-coupled differential pair can be recognized as negative resistors.

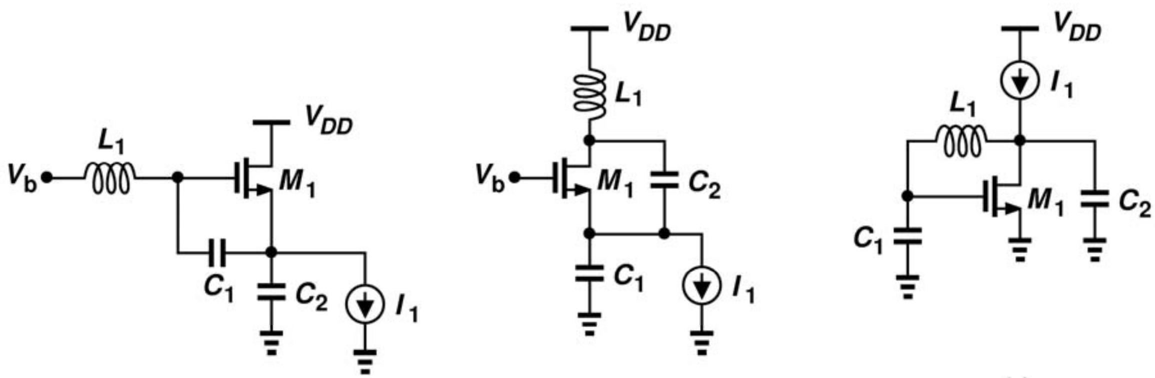




One Port Oscillators

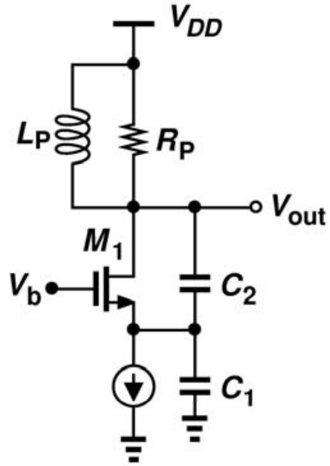


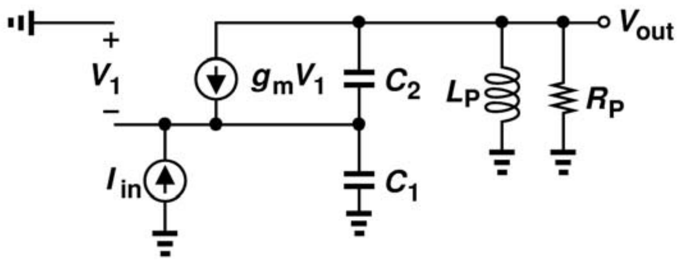
- Three possible realizations



- As long as a negative equivalent resistance can be found, an oscillator can be made.

Colpitts Oscillator





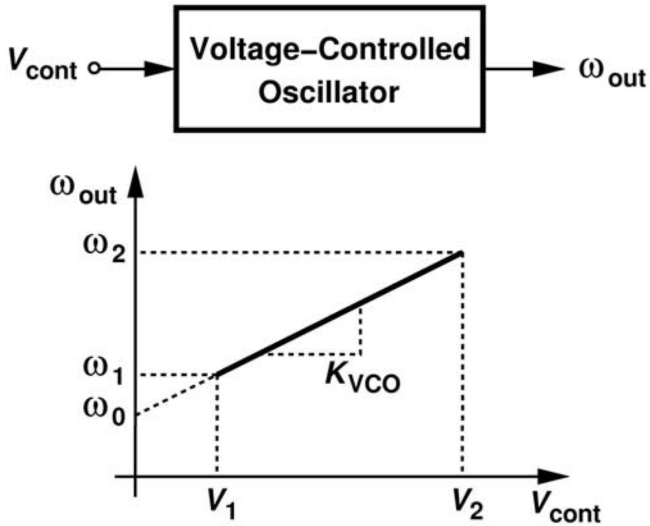
$$\frac{V_{out}}{I_{in}} = \frac{R_p L_p s (g_m + C_2 s)}{R_p C_1 C_2 L_p s^3 + (C_1 + C_2) L_p s^2 + [g_m L_p + R_p (C_1 + C_2)] s + g_m R_p}$$

$$g_m R_p = \frac{C_1}{C_2}(1 + \frac{C_2}{C_1})^2 \geq 4 \quad (@\, C_1 = C_2)$$

$$\omega_R = \frac{1}{\sqrt{L_p (C_p + \frac{C_1 C_2}{C_1 + C_2})}} \quad \text{(if } C_p \text{ included)}$$

- ❒ **Oscillates under proper conditions.**

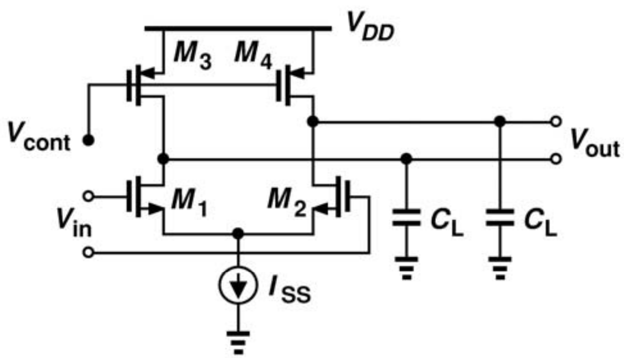
Voltage-Controlled Oscillator

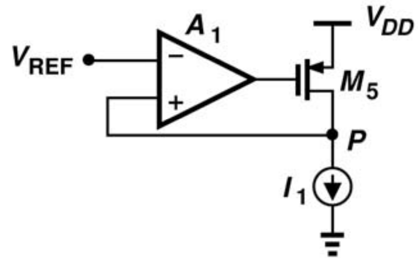


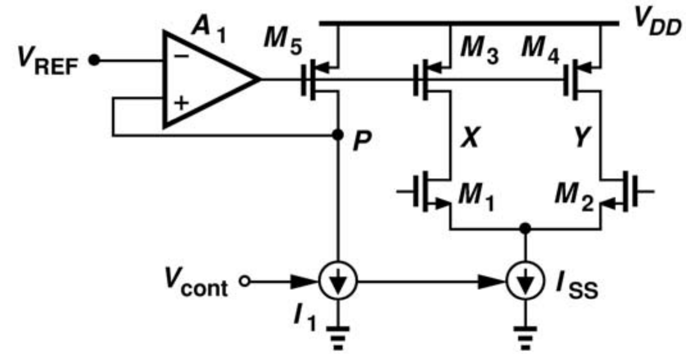
Tradeoffs:

- ❒ Center Frequency
- ❒ Tuning Range
- ❒ Power Dissipation
- ❒ Phase Noise
- ❒ Tuning Linearity
- ❒ Output Amplitude
- ❒ Supply Rejection

Ring VCO – Output Swing Control

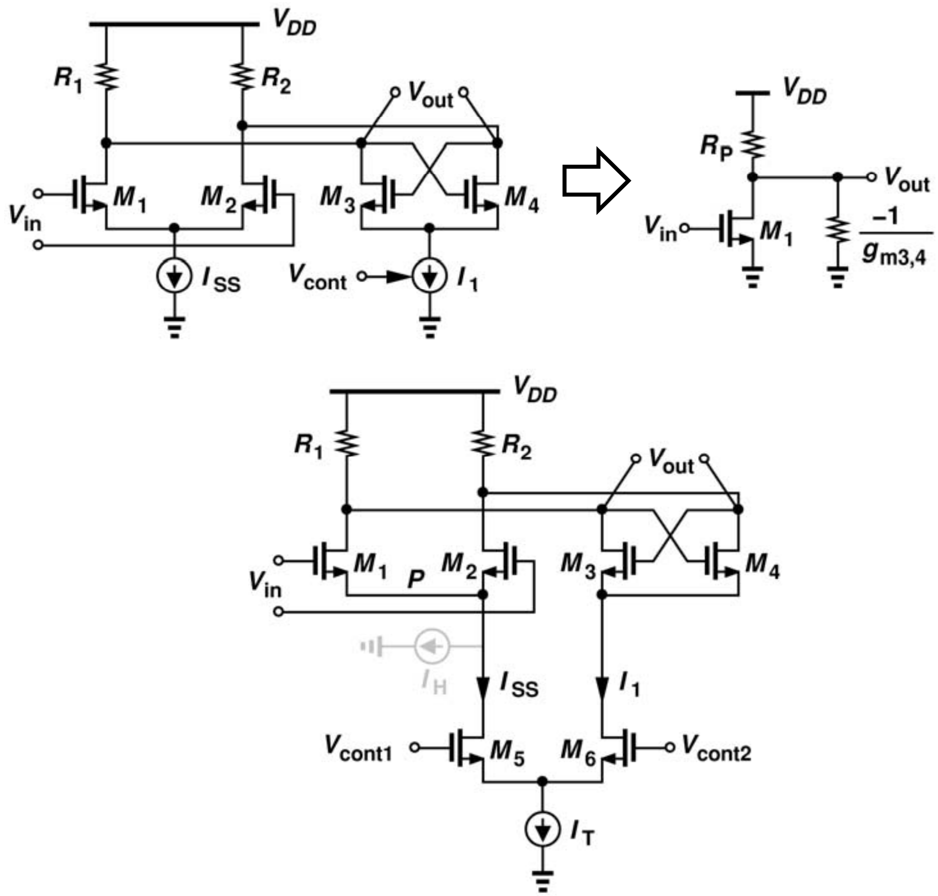






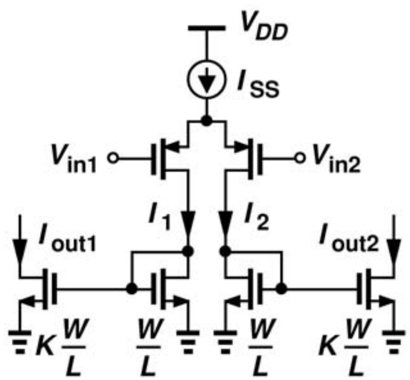
- Replica biasing "servos" the on-resistance to vary the frequency while maintaining the constant output swing.

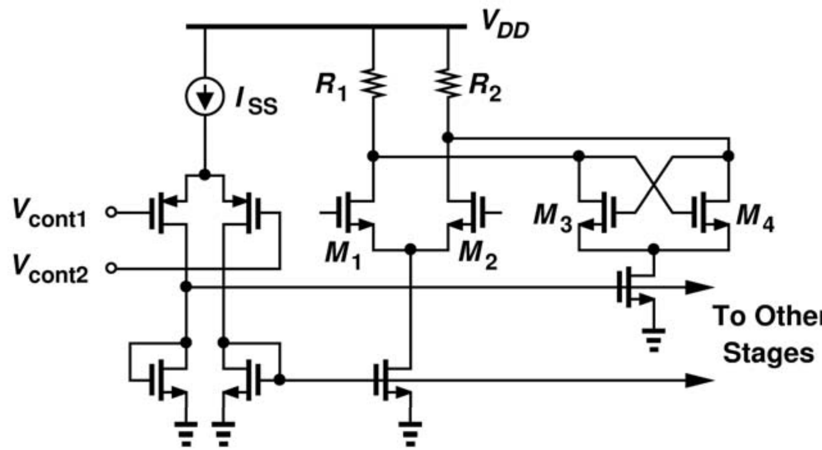
Ring VCO – Delay Variation by Positive Feedback



- Current steering topology keeps the swing constant.
- It may suffer from voltage headroom issue.

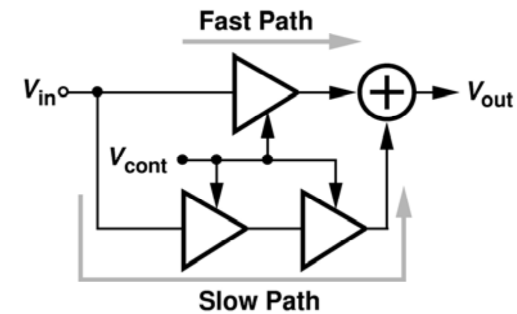
Ring VCO – Current-Folding Topology

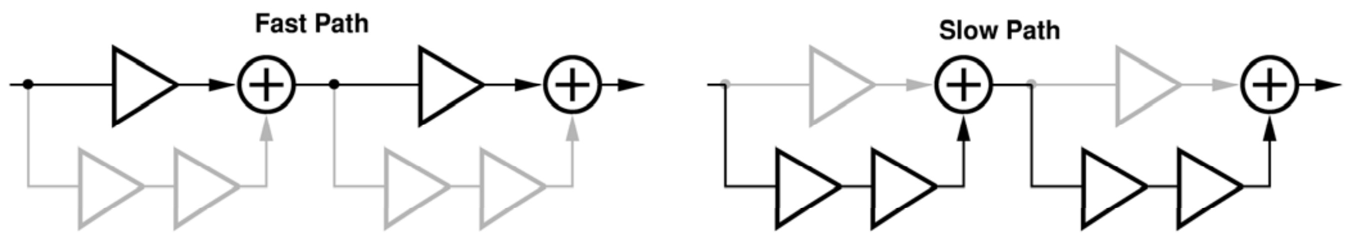


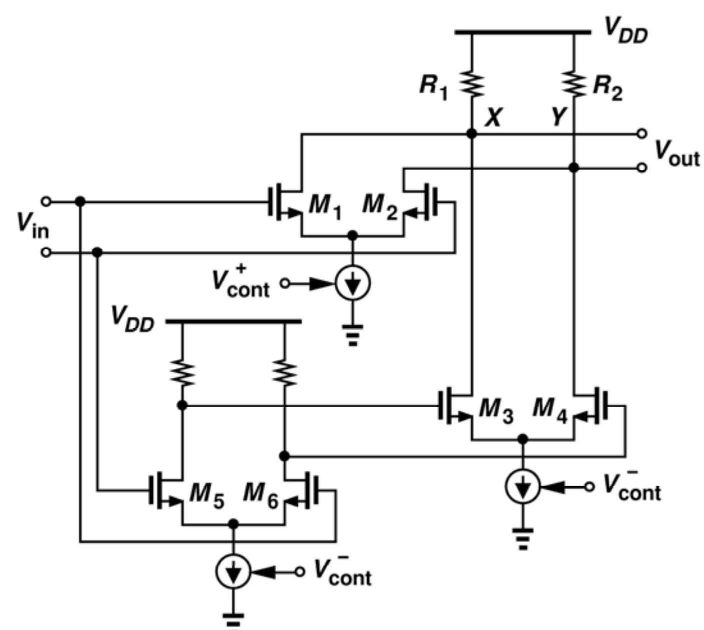


- Folding the current saves one stacking stages.

Ring VCO – Delay Variation by Interpolation

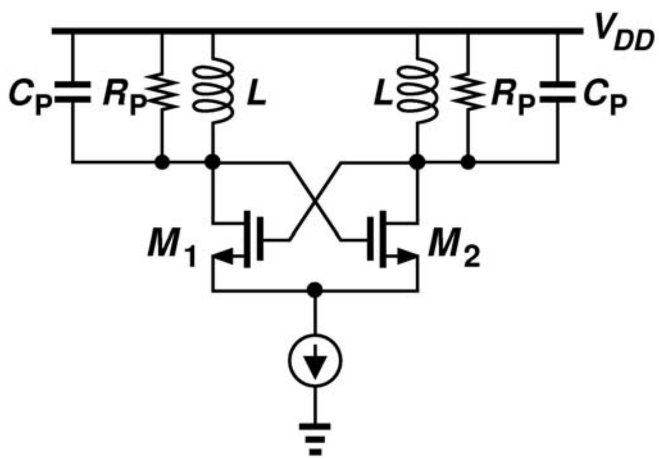


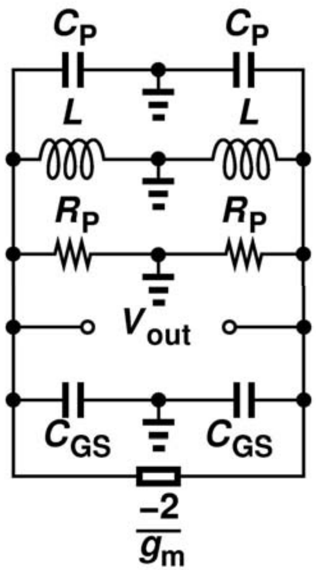




- Stability issue?
- Large tuning range

Oscillation Frequency of Simple LC Oscillator





$$R_p = Q \cdot \omega_{osc} L = 1/g_m$$

$$\omega_{osc} = \frac{1}{\sqrt{2L\left(\frac{C_p}{2} + \frac{C_{GS}}{2}\right)}}$$

Oscillation Frequency of LC Oscillator

- If C_p is insignificant compared with C_{GS}, then

$$\omega_{osc} \approx \frac{1}{\sqrt{LC_{GS}}} = \frac{1}{\sqrt{\frac{1}{g_m Q \omega_{osc}} C_{GS}}} = \sqrt{Q \omega_T \omega_{osc}}$$

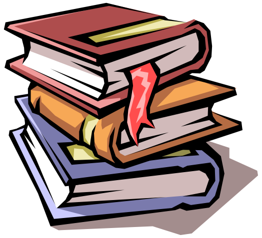
$$\Rightarrow \omega_{osc} = Q \cdot \omega_T$$

- An LC oscillator could theoretically operate at arbitrarily high frequency as long as the inductor provides a sufficiently high Q.
- In reality, neither C_p is negligible nor can an on-chip inductor achieve very high Q, nor negligible C_p.

Oscillators (II)

Professor Jri Lee

台大電子所　李致毅教授

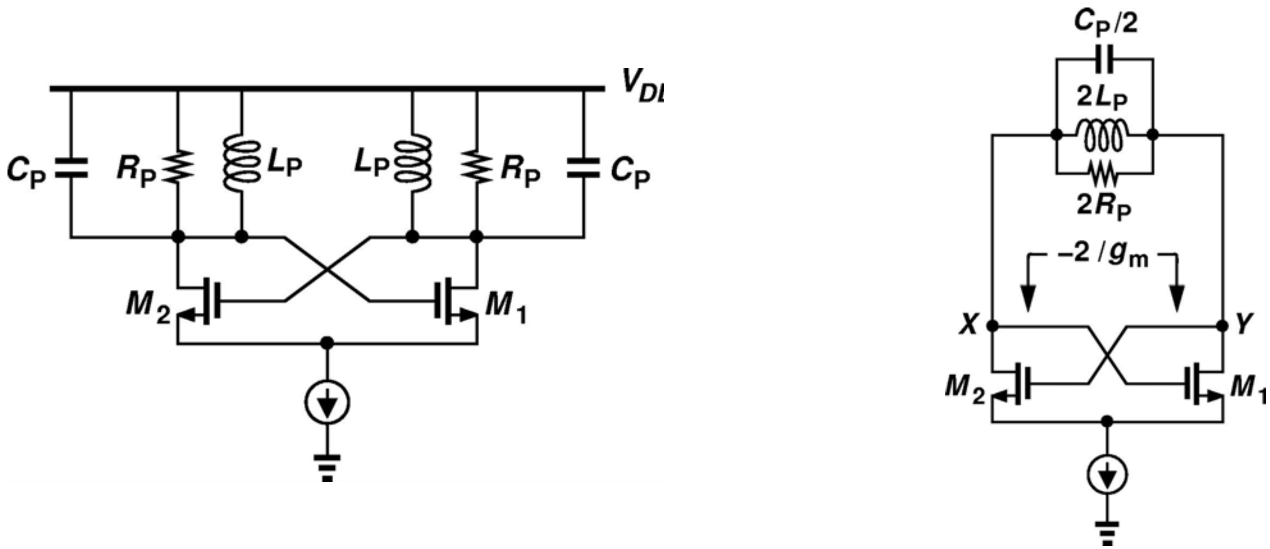


Electrical Engineering Department
National Taiwan University

Outlines

- General Considerations
- Inductor Designs
- Varactor Designs
- Quadrature Oscillators
- Distributed Oscillators

Basic LC Oscillators



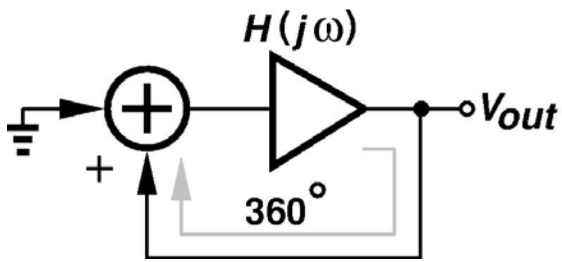
- Cross-coupled pair provides negative resistance to compensate inductor loss.

Advantages:

- Large Swing
- Higher Frequency
- Low Supply Voltage
- Lower Phase Noise

Operation Theory

Barkhausen Criteria:

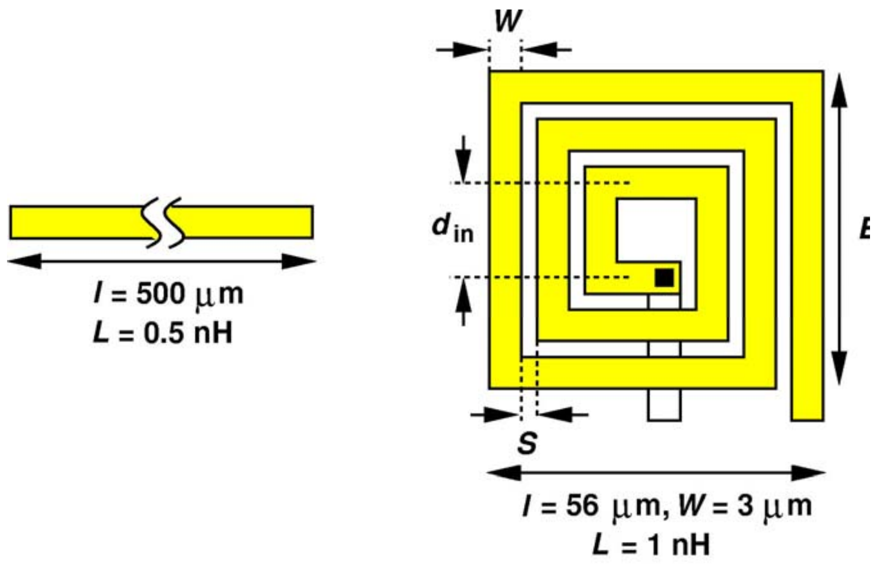


$$|H(j\omega)| \geq 1$$

$$\angle H(j\omega) = 360^\circ$$

- Necessary but not sufficient conditions.
- Require 2~3 times larger loop gain to ensure oscillation.

Monolithic Inductors



- Inductance calculation involves EM field equations.
- Spiral turns achieve higher inductance by mutual coupling between turns.
- Optimum values of inductance, parasitics, and *Q* require reiterative designs with software simulations.

Inductor Loss Mechanisms

❐ **Ohm Loss**

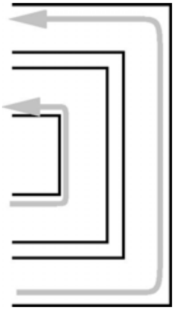
⇒ **Arises from the series resistance of the metal wire: comprising the spiral.**

⇒ **Modern VLSI technologies provide a sheet resistance of 20 to 70 mΩ/ □.**

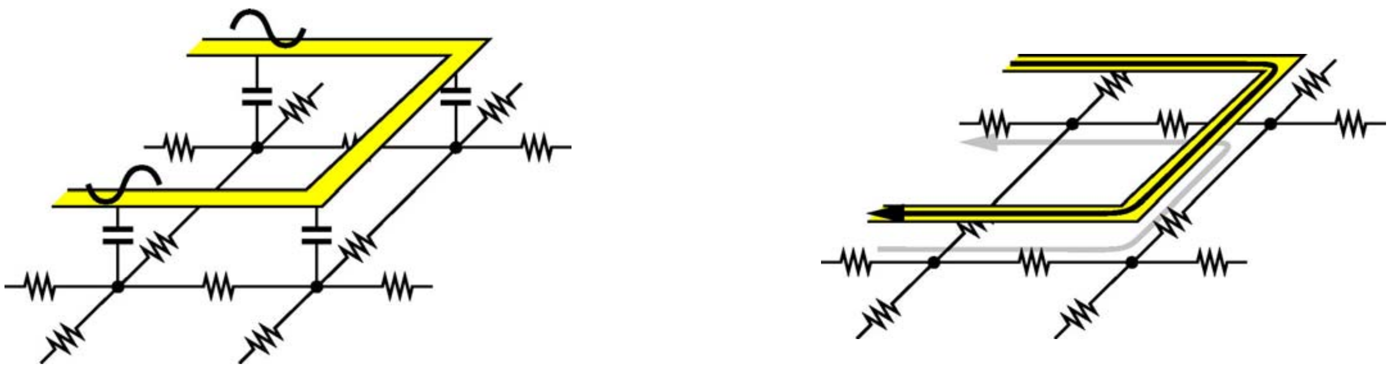
❐ **Skin Effect**

⇒ **Current tends to concentrate on the edge at high frequencies, changing the magnetic flux and the inductance.**

⇒ **Inductor *Q* decreases as well.**



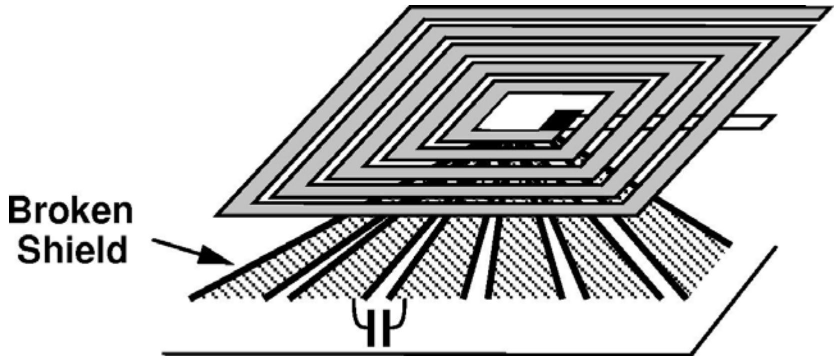
Losses due to Capacitive and Magnetic Coupling



- Finite substrate resistance results in loss.
- A high-resistance (i.e., lightly-doped) substrate minimizes the loss in both cases.

Inductor Design Techniques

❒ **Ground Shield**

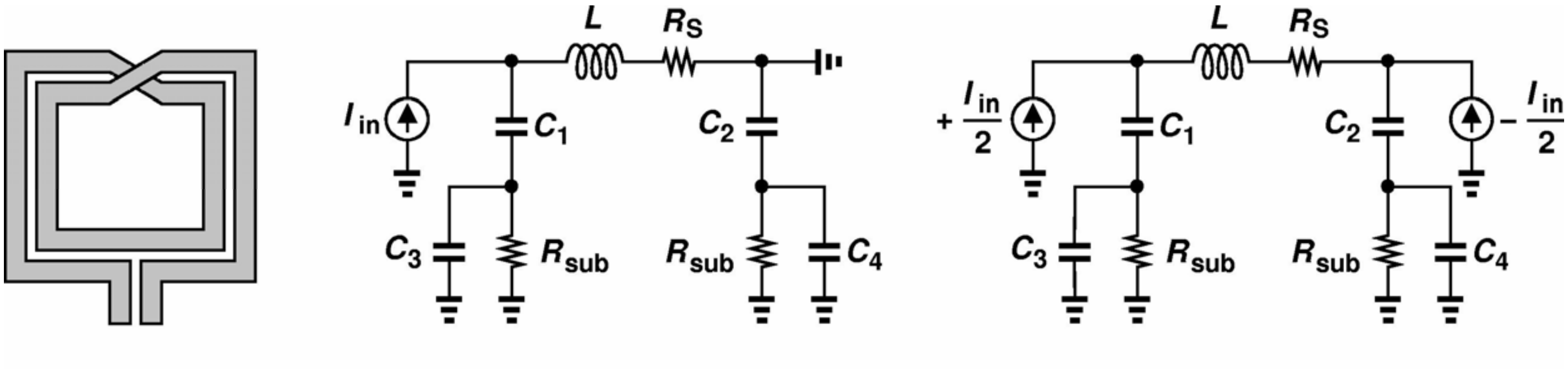


⇒ **Isolate the substrate from capacitive coupling.**

⇒ **Eddy current is reduced as well since a large portion of EM field lines terminates at ground shield.**

Inductor Design Techniques

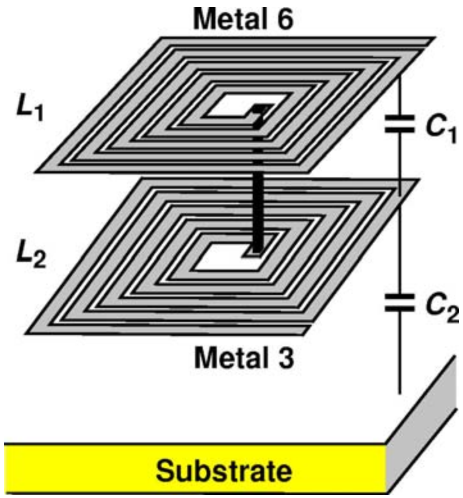
- Differential Structures



⇒ **Improve *Q* by reducing the substrate loss.**

Inductor Design Techniques

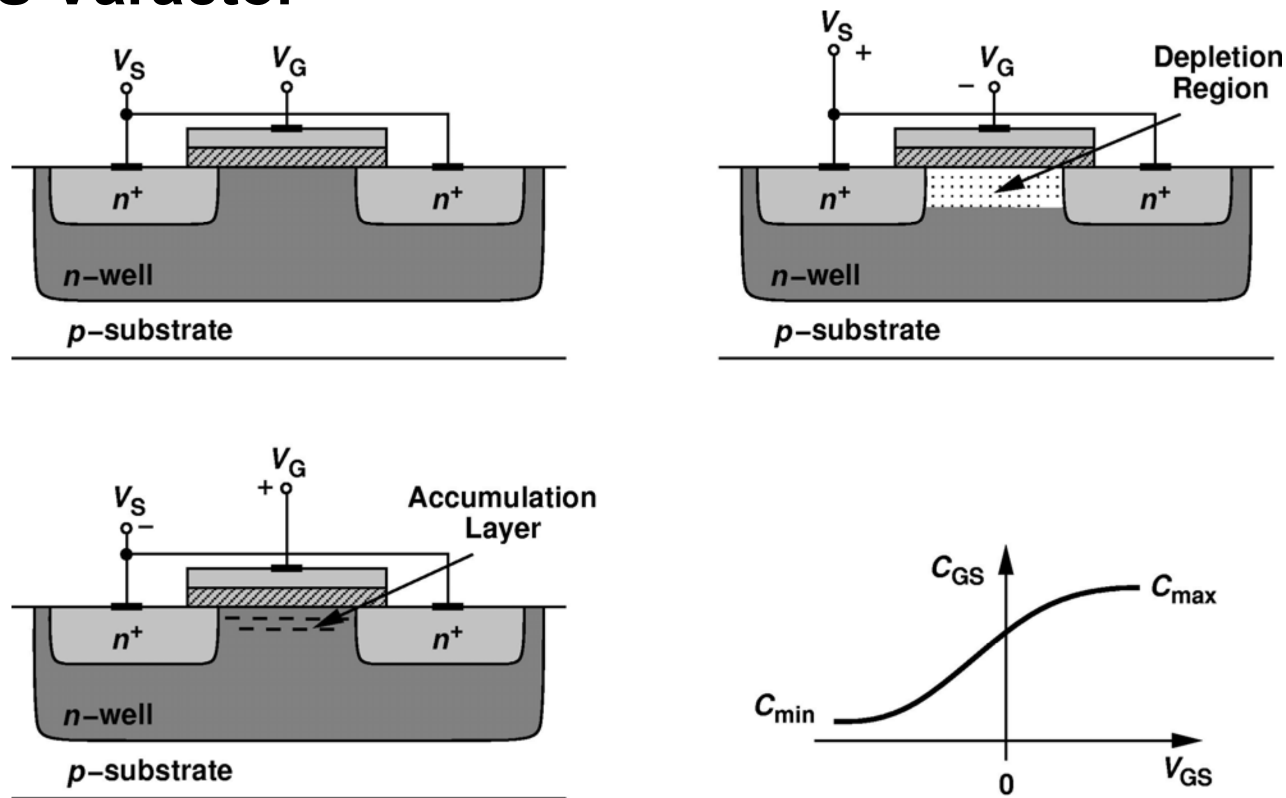
❒ **Stacked Structures:**



$\Rightarrow$ **Increase the self-resonance frequency by lowering the equivalent capacitance.**

Monolithic Varactors (I)

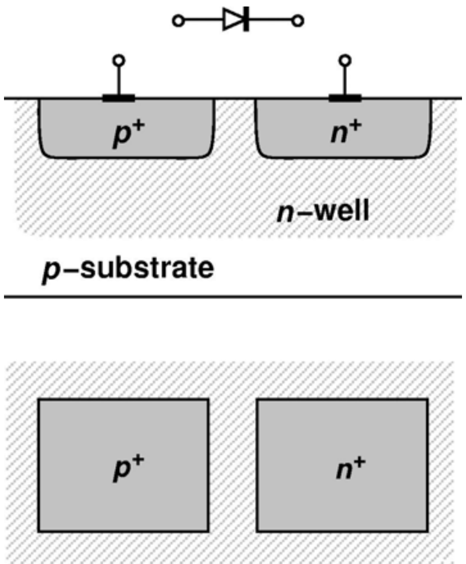
- MOS Varactor

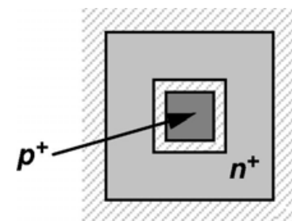


- C_{GS} presents a monotonic variation with a dynamic range of 2~3 times.

Monolithic Varactors (II)

- Reverse-Biased pn Junction

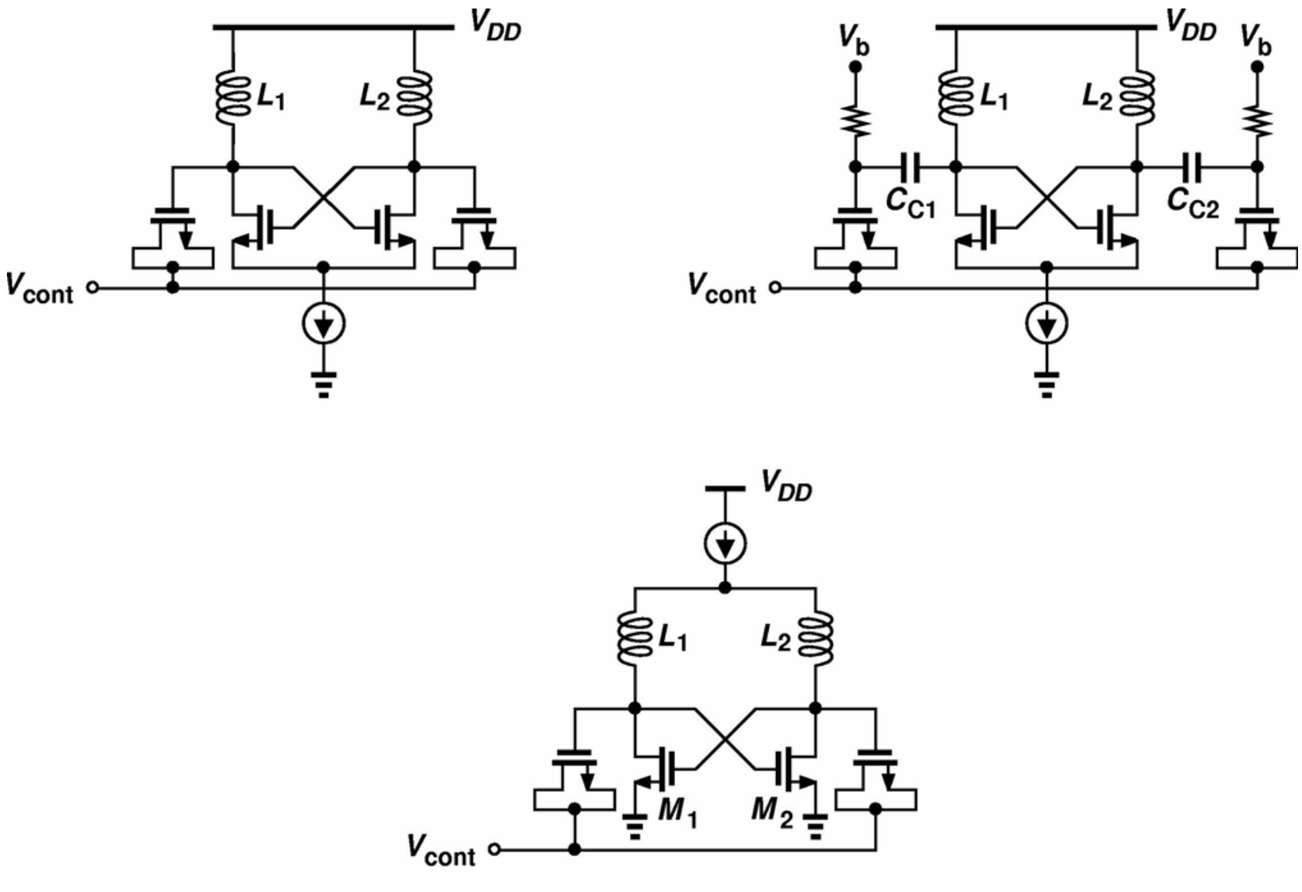




$$C_{var} = \frac{C_0}{\left(1+\frac{V_R}{\phi_B}\right)^m}$$

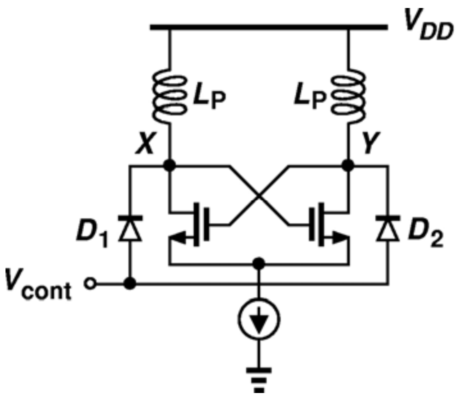
- Approximately 2-2.5 times variation range.

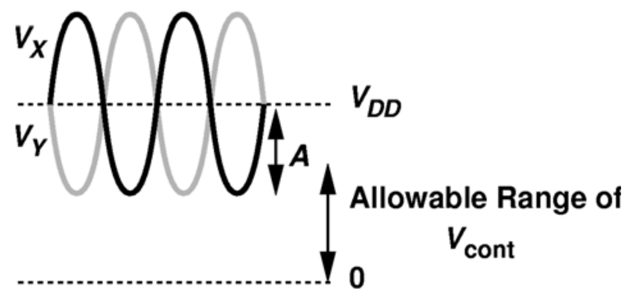
VCO with MOS Varactors

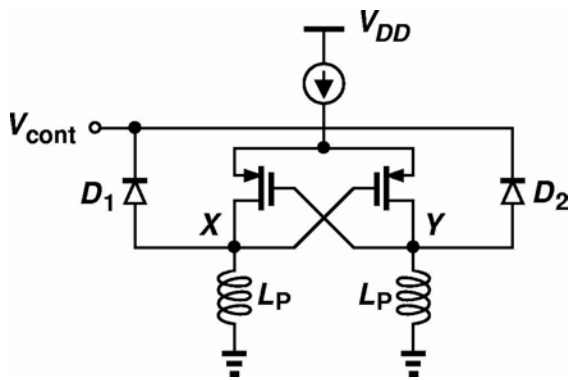


- VCO with current source on top maximize the tuning range. (Why?)

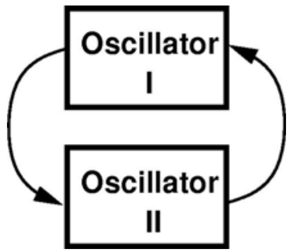
VCO with pn-Junction Varactors

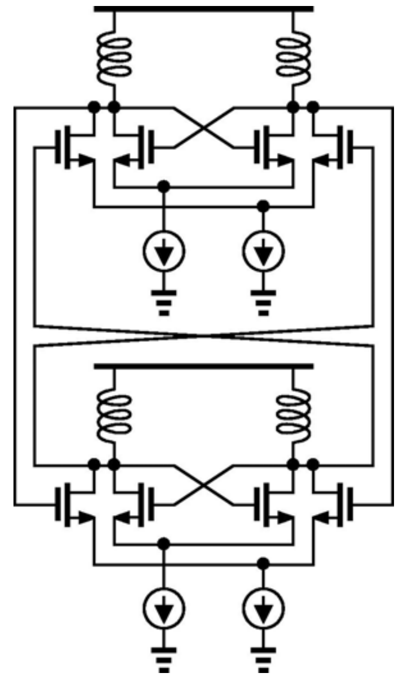






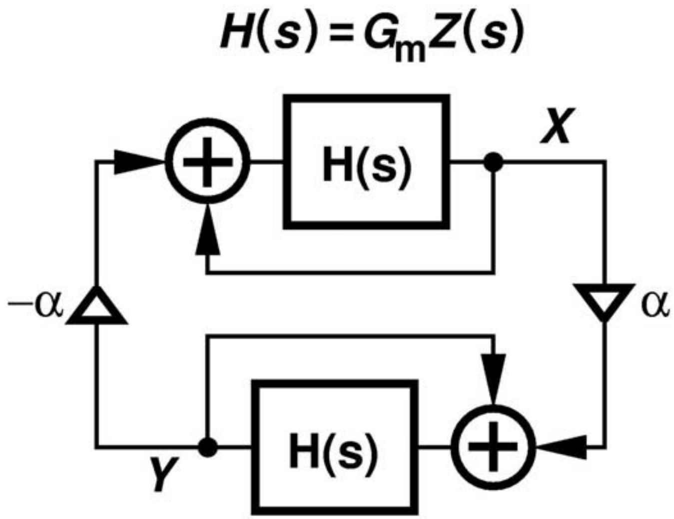
Quadrature Oscillators





- Two identical oscillators coupled together to create quadrature outputs.

Quadrature LC VCO Analysis

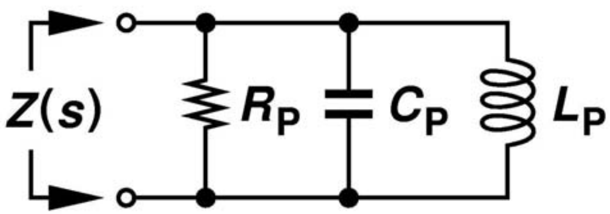


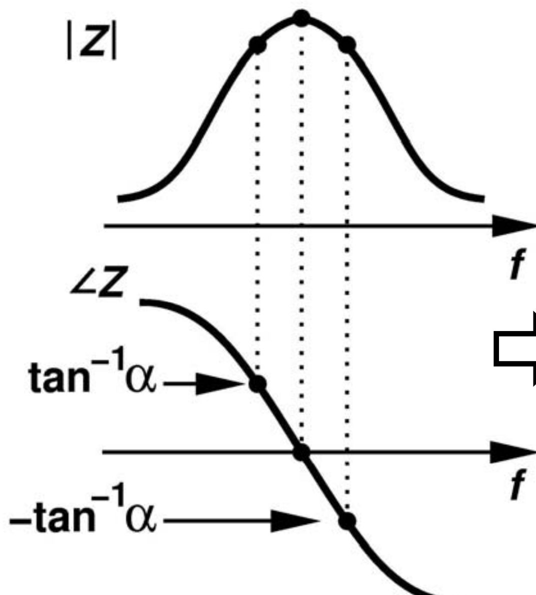
$$(-\alpha Y + X)H(s) = X$$

$$(-\alpha X + Y)H(s) = Y$$

$$\Rightarrow X^2 + Y^2 = 0$$

$$\Rightarrow \mathbf{X} = \pm jY, \quad \angle H(s) = \pm\tan^{-1}\alpha$$

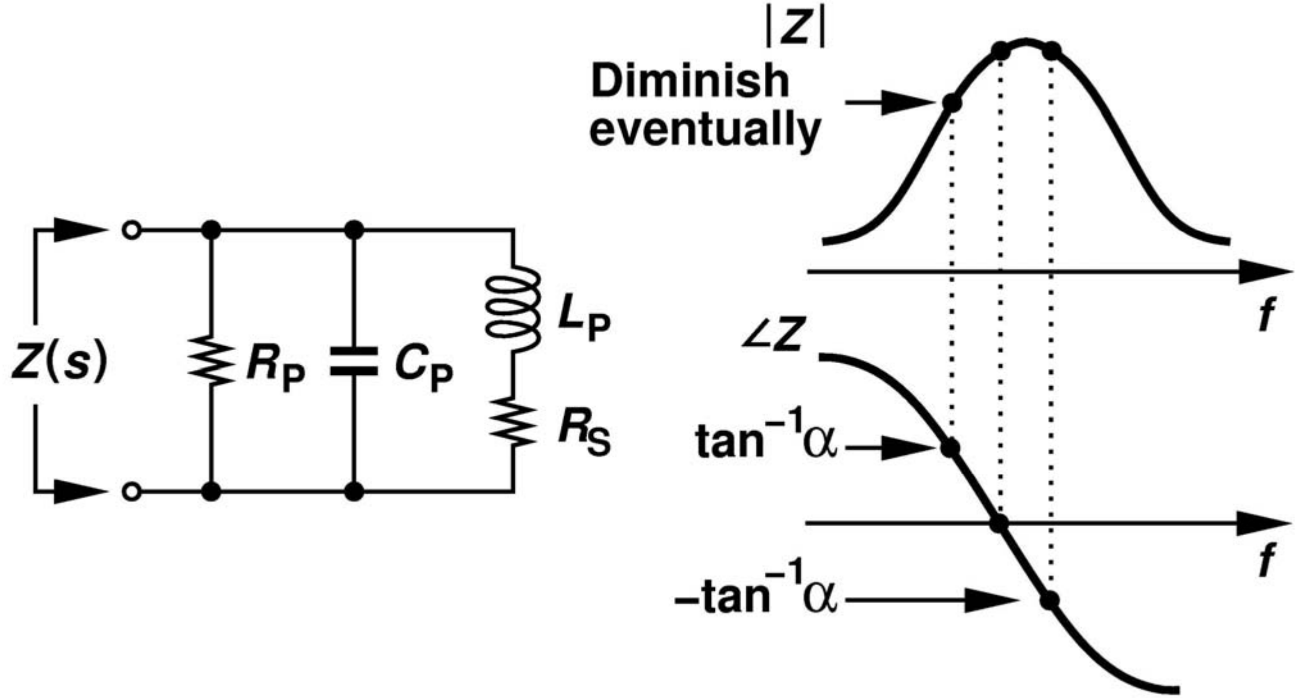




⇨ Frequency Ambiquity!

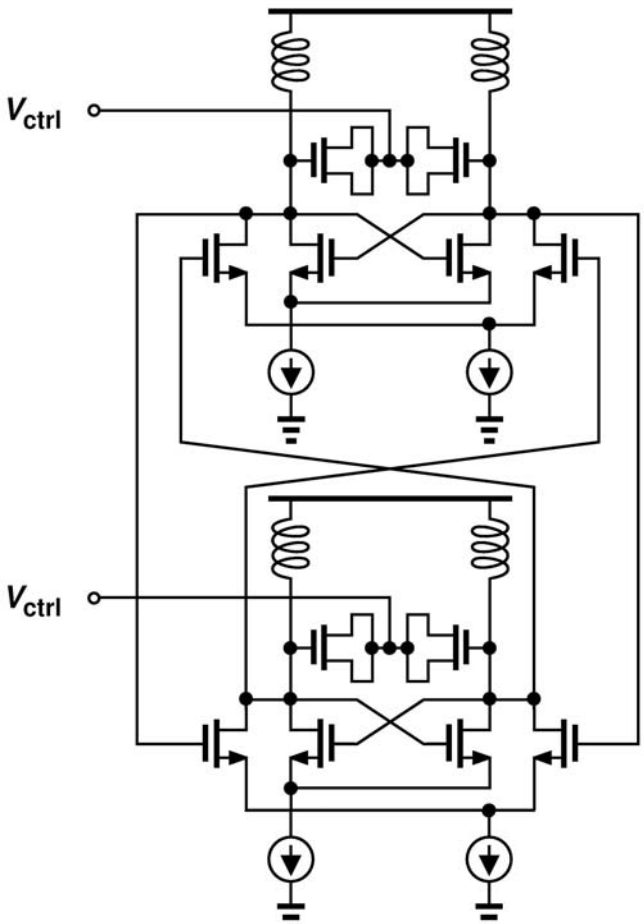
Quadrature LC VCO Analysis

- **Actually a series resistance R_S must be incorporated to model the Ohm loss at low frequencies.**
- **System adjusts itself to have only one solution; the other diminishes due to insufficient loop gain.**

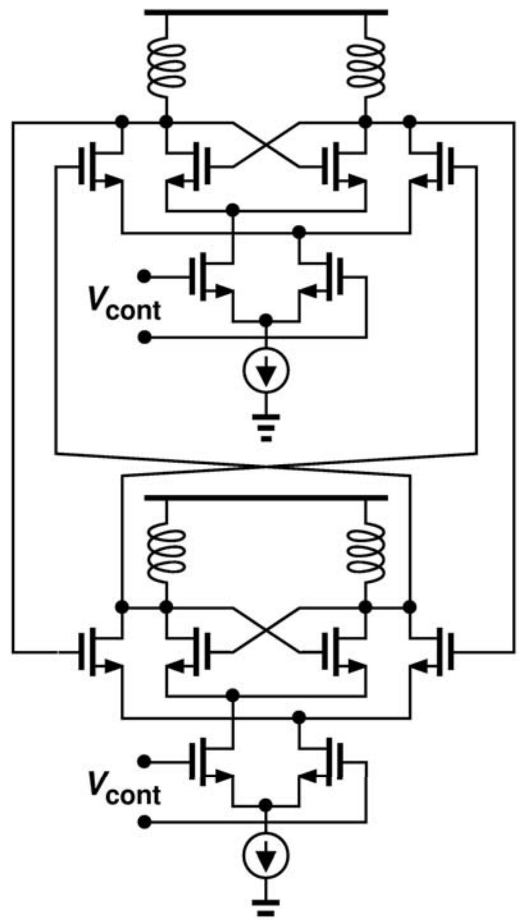


Quadrature VCO Tuning

Varactor Tuning



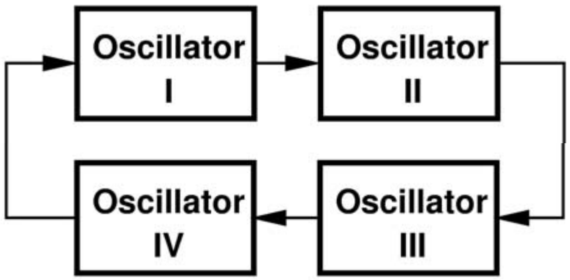
Bias-Current Tuning



- Tuning can be achieved in different ways.

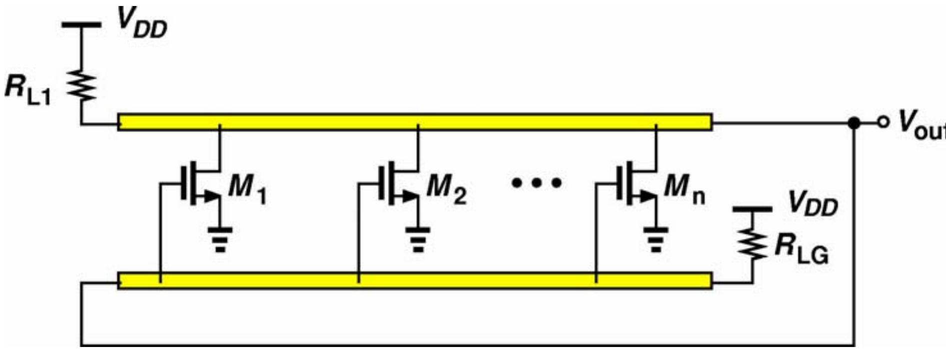
Drawbacks of Quadrature VCO

- May still be prone to frequency ambiguity under mismatches.
- Operating away from the resonance of the tank; raising the phase noise.
- May lose quadrature phase locking if the coupling factor between oscillators becomes too small.
- Nonetheless, it is still popular and can be extended to semi-quadrature operation.



- Semi-quadratre is also possible.

Distributed Oscillators

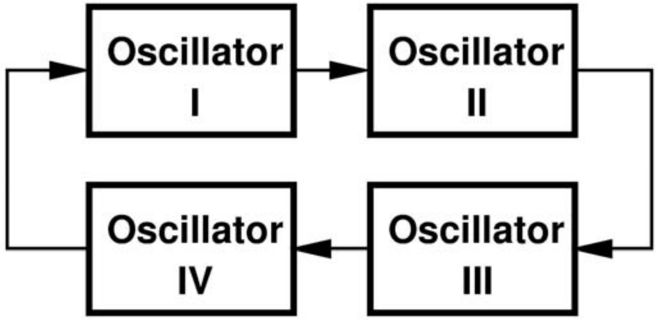


$$A_V = \frac{\pi f_T}{2 f_{osc}}$$

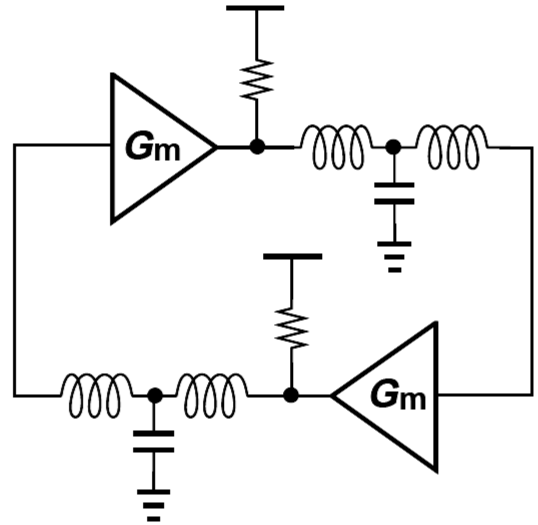
$$f_{osc} = \frac{\pi f_T}{2}$$

- Difficult to achieve multiphase operation due to unequal amplitudes.

LC VCO Topologies



(Kim & Kim, ISSCC ’00)

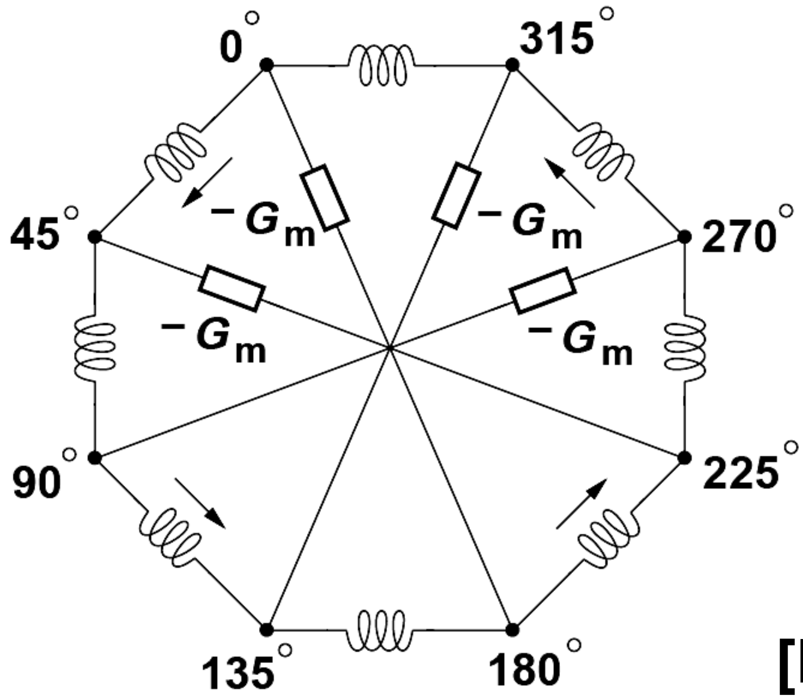


(Rogers & Long, ISSCC ’02)

- Operates away from tank resonance.
- Requires knowledge of tank Q and oscillator mismatches to set the coupling factor.

- Resistors dissipate energy in each cycle.

Case Study (I)



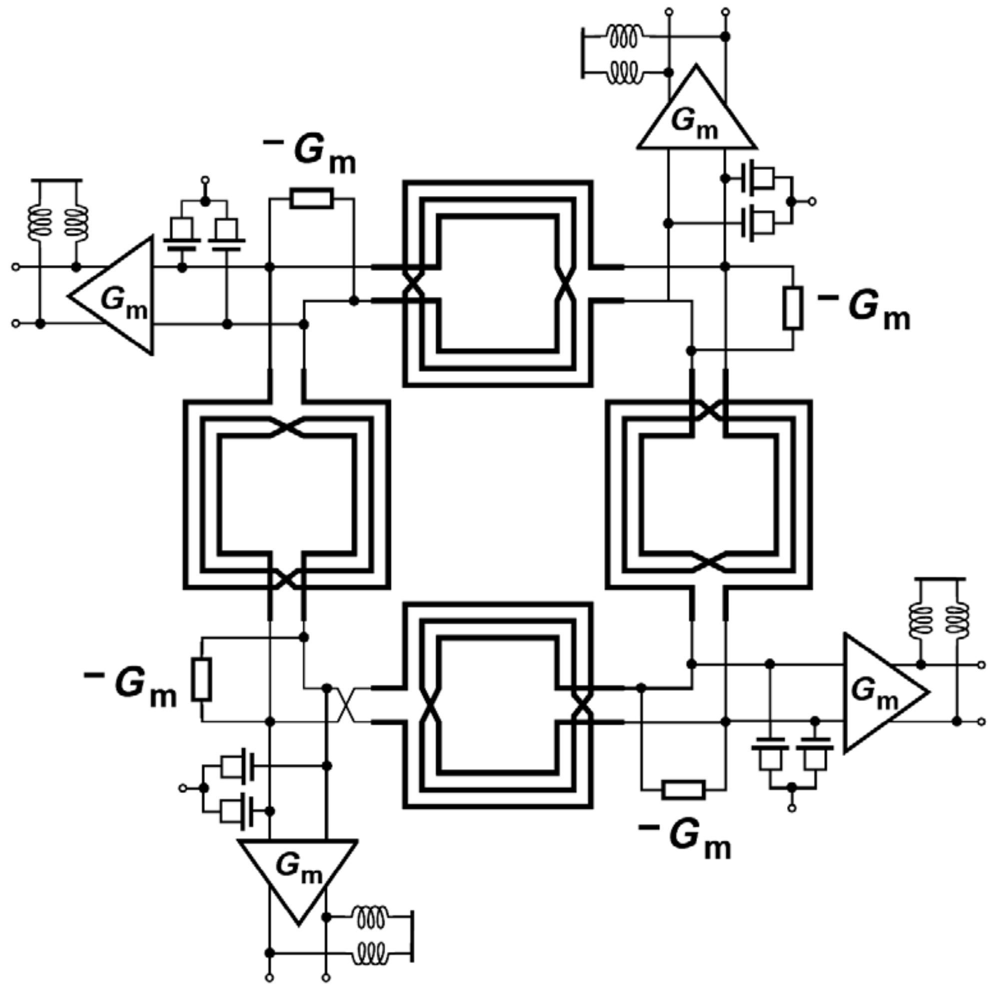
[Lee, '03]

- Operates at line resonance frequency:

$$f_{osc} = \frac{1}{8\sqrt{L_u C_u}}$$

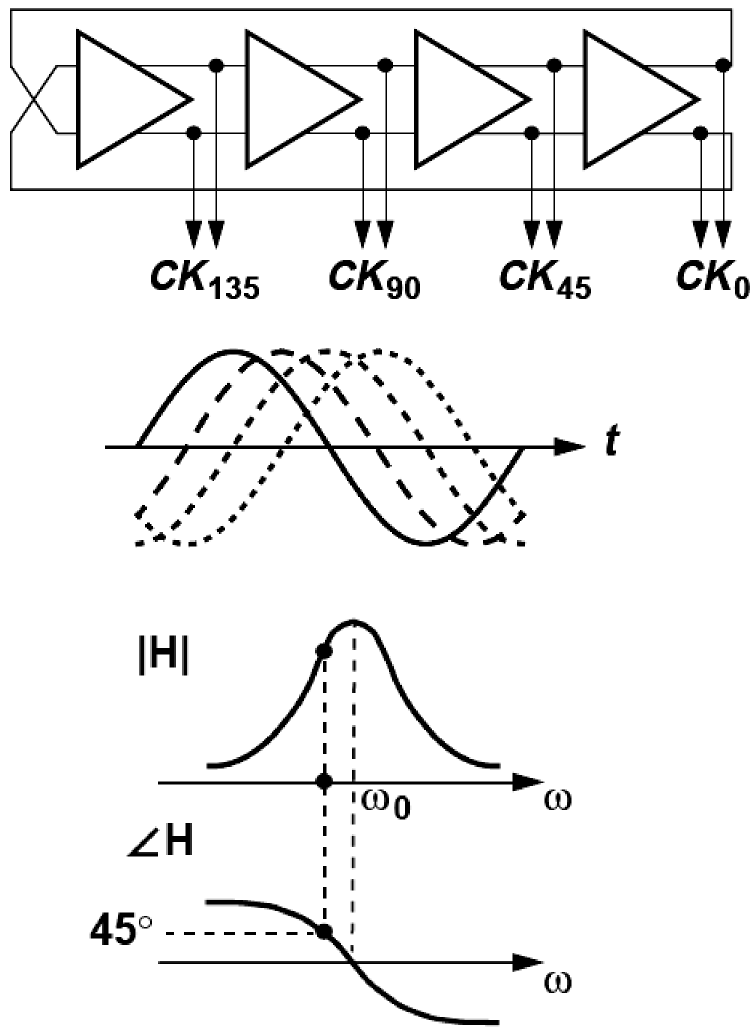
- Self−terminated −> requires no termination resistors.
- But routing signals to −Gm stages requires long interconnects.

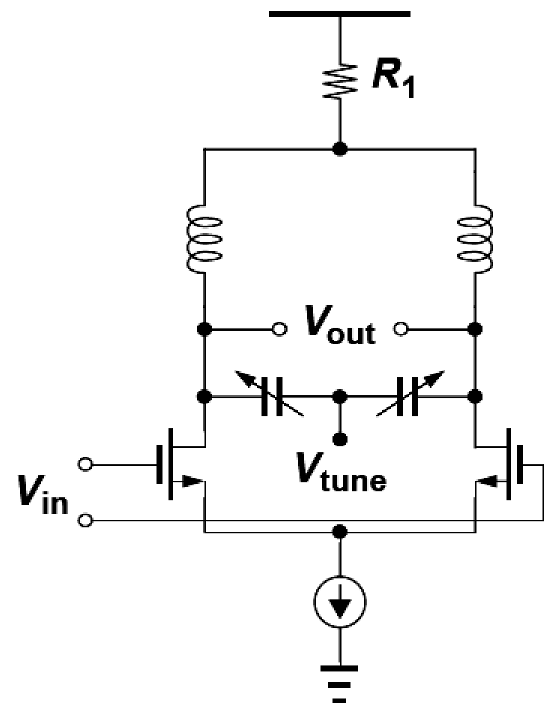
Case Study (I)



- Inductively−loaded buffers:
  - Isolate VCO from data edges in PD.
  - Provide swings above V_{DD}.

Case Study (II)



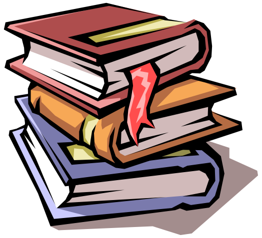


[Savoj, '01]

Frequency Dividers

Professor Jri Lee

台大電子所　李致毅教授



Electrical Engineering Department

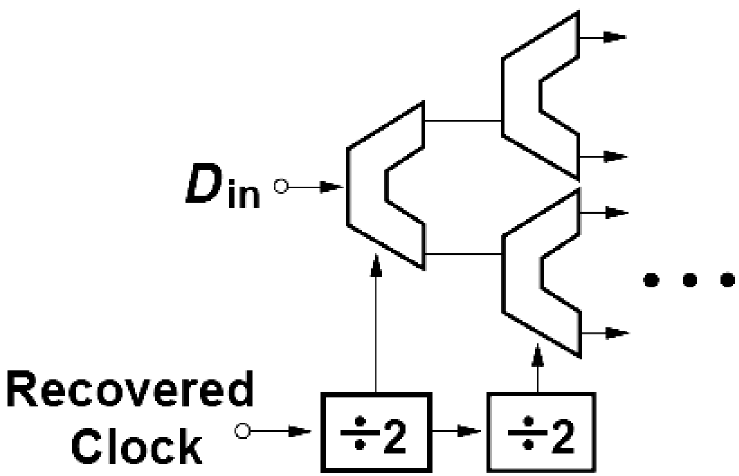
National Taiwan University

Outline

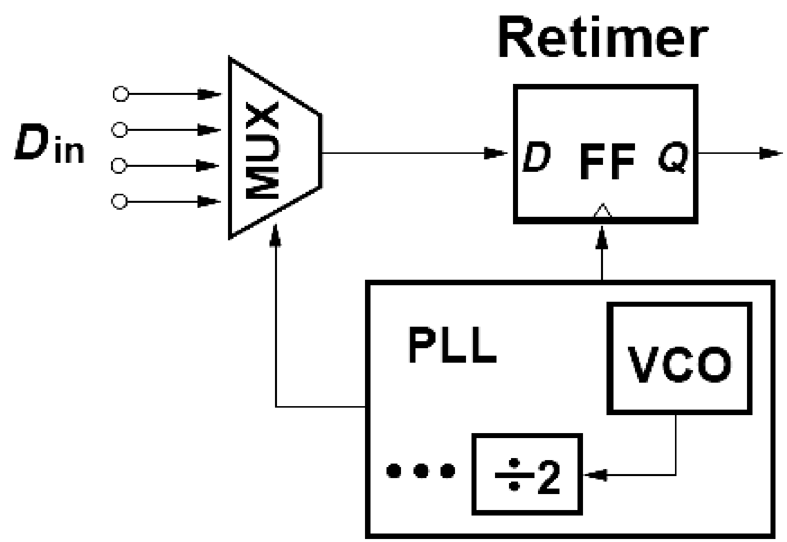
- Introduction
- Static Dividers
- Miller Dividers
- Injection Dividers
- Prescalers
- Case Study

Full-Rate Divider Applications

Broadband Receiver



Broadband Transmitter

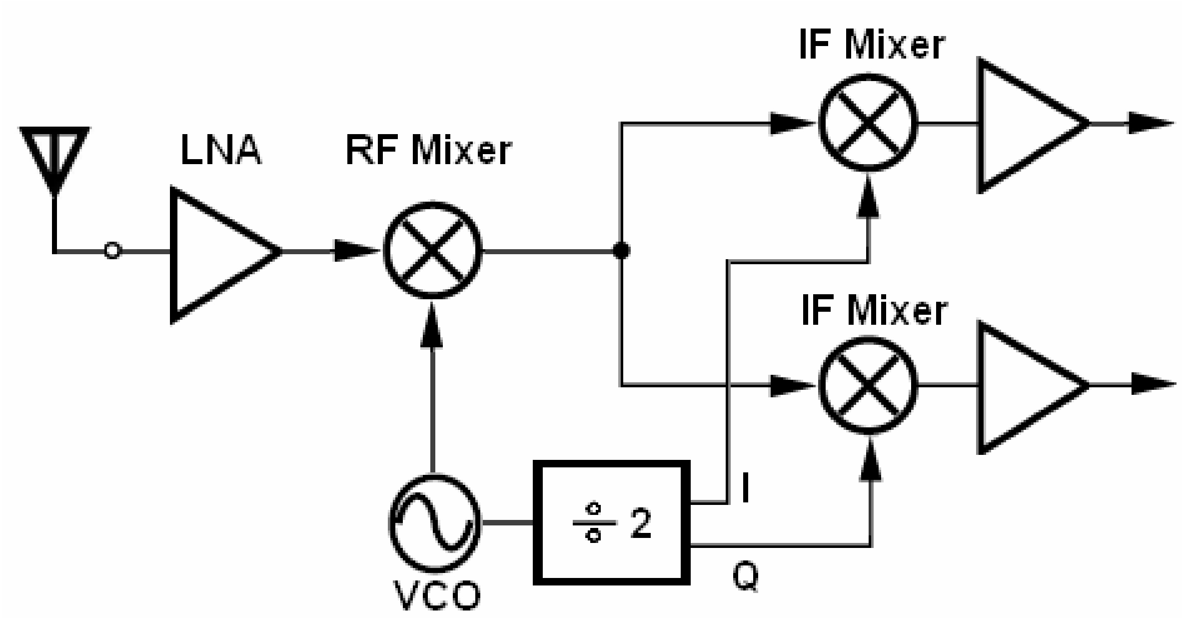


- Half−rate retimer in transmitter would be prone to clock and device asymmetries

  => Must use a full−rate retimer.
  => Need a 40−GHz divider.

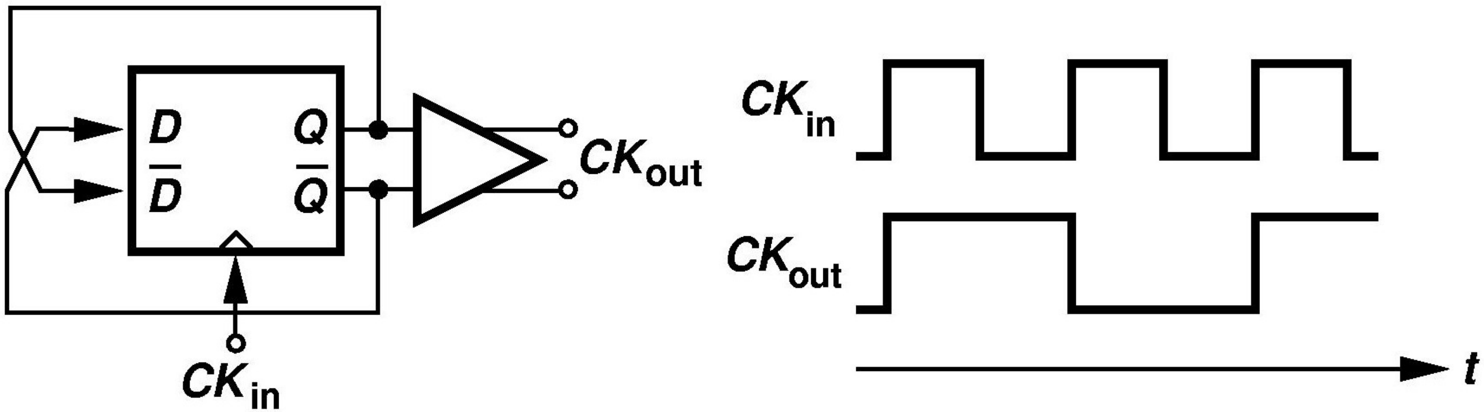
Full-Rate Divider Applications

Wireless Frontend



- I/Q mismatch of great importance.
- Very high speed.

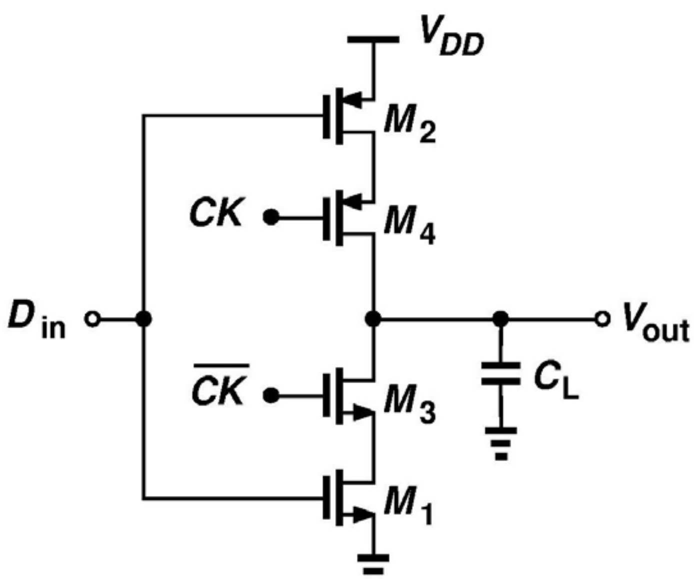
Static Dividers

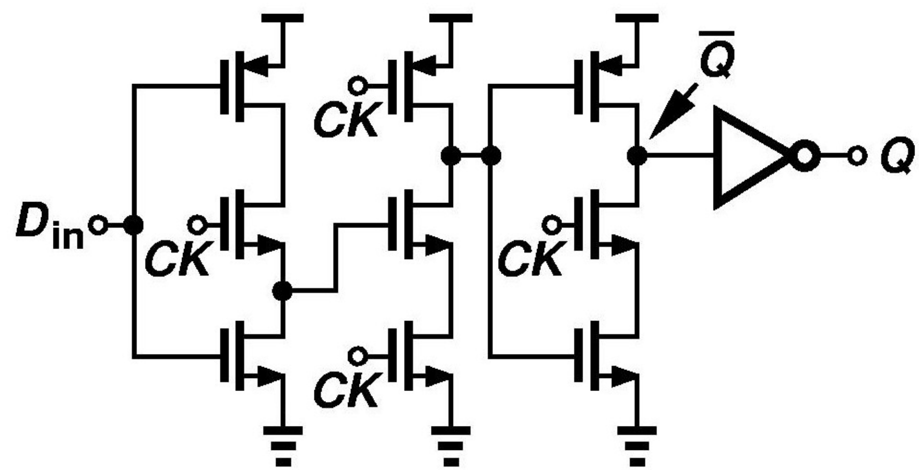


- Edge-triggered flipflop toggle between the two states by "negative feedback".
- Wide range of operation (almost from DC to the circuit's bandwidth).
- Overlapped clock may cause racing.
  ⇨ Rising/falling time of CK_{in} matters.

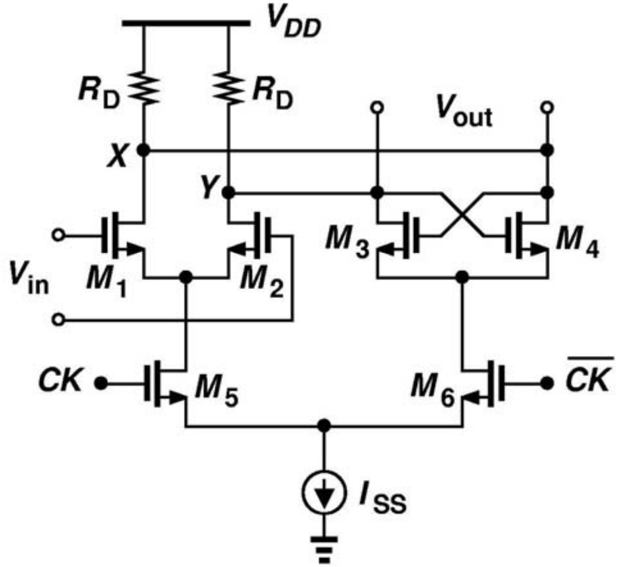
Implementation of Flipflops

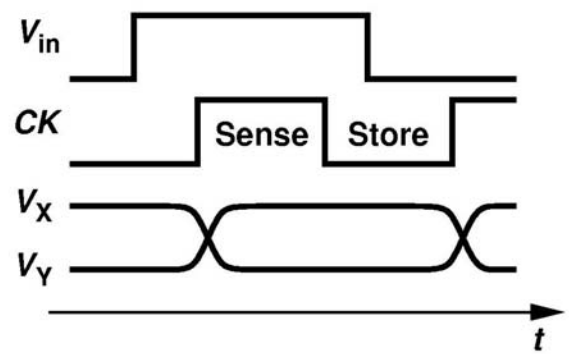
- **Almost any type (digital or analog) can serve:**
  - **Multiplexer-Based**
  - **Pseudostatic**
  - **C^2MOS**
  - **TSPC**
  - **CML (Current-Steering)**

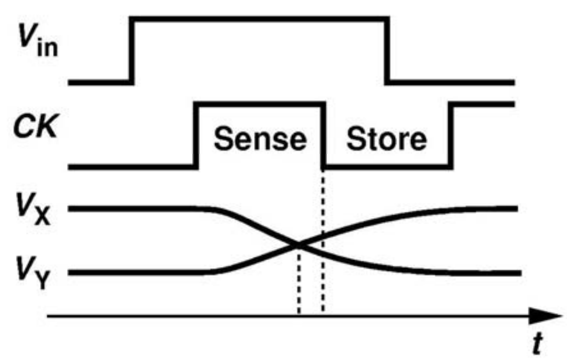




CML Latch

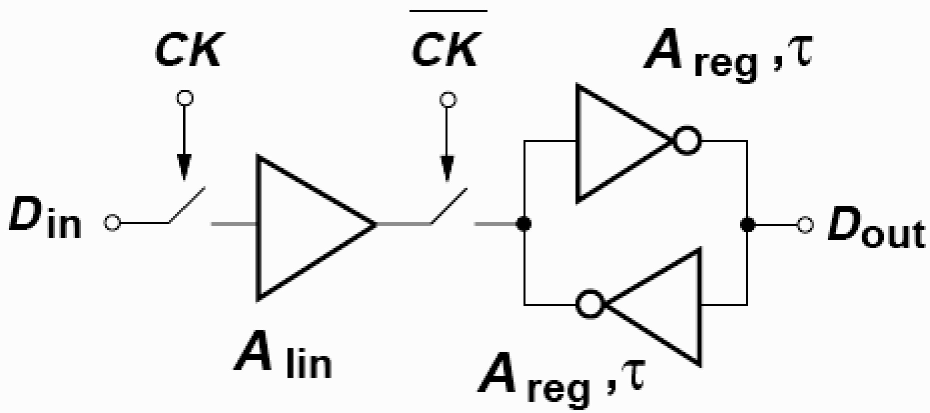






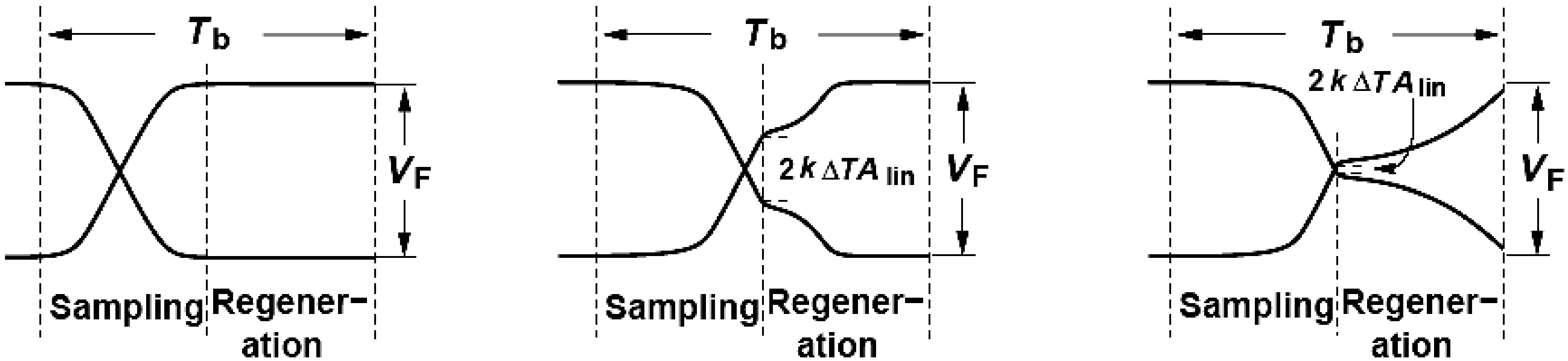
- Speed limited by *RC* time constant.

Meta-Stability



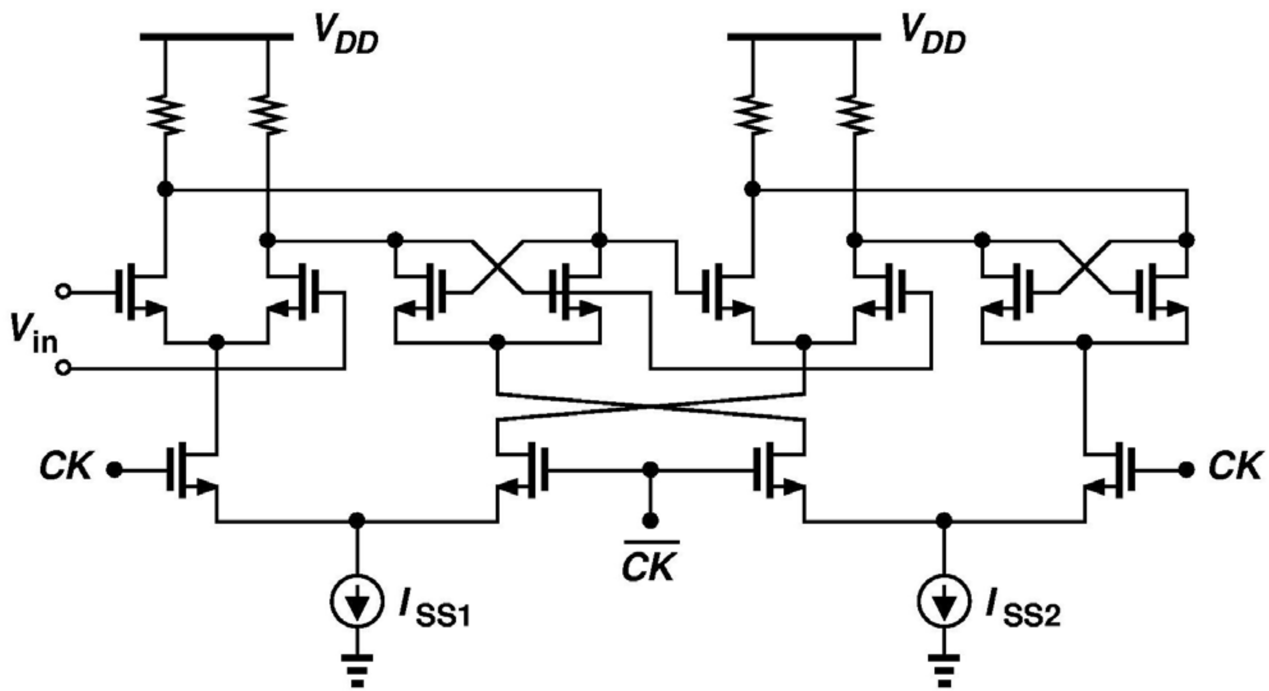
- Metastable sampling may cause incomplete regeneration, leading to a finite slope at small $\Delta\phi$.
- Depends on linear gain A_{lin}, regeneration gain A_{reg}, and time constant τ.

Regeneration of Meta-Stable Points



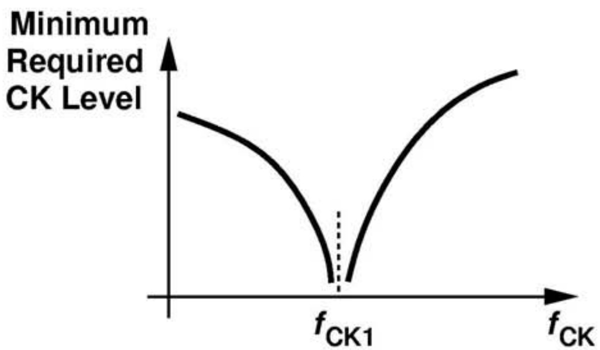
- FF-based divider fails when it can not flip the state in one (input) clock cycle.

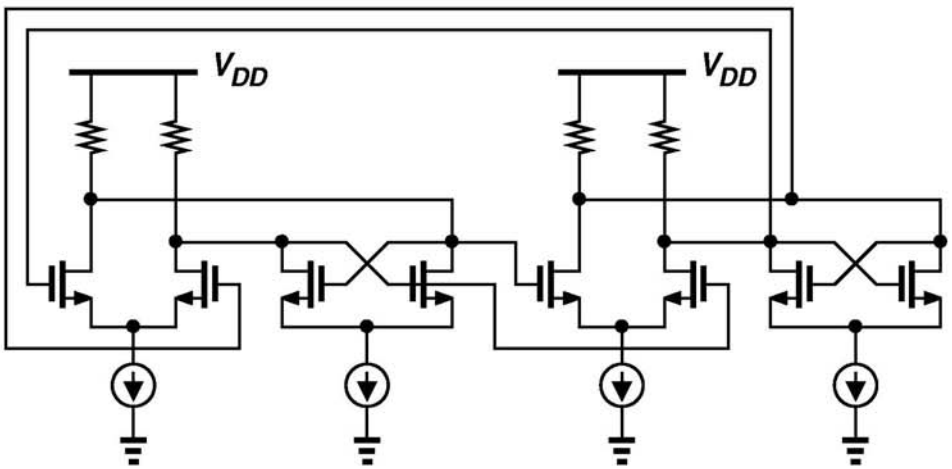
Superdynamic Flipflop



- Allows different current for sampling and regeneration.

Free-Running Frequency

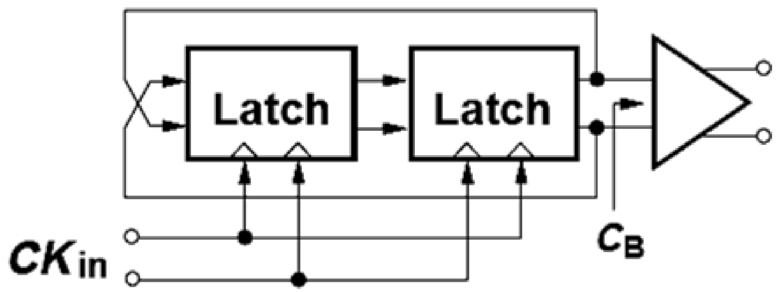




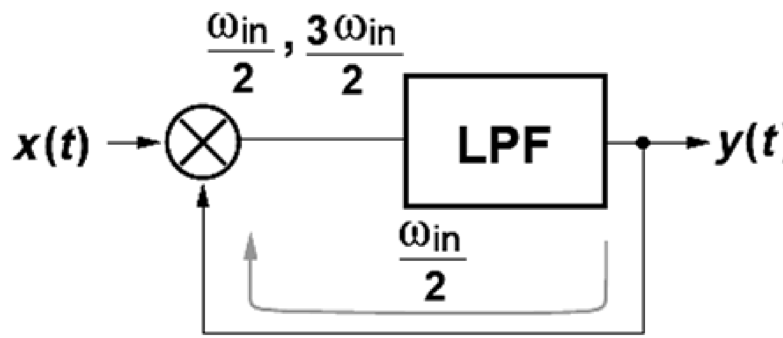
- At f_{CK1} the divider behaves as a ring oscillator (with the cross-coupled pair providing sufficient phase shift), and requires little input power.

Static and Dynamic Dividers

Static Divider

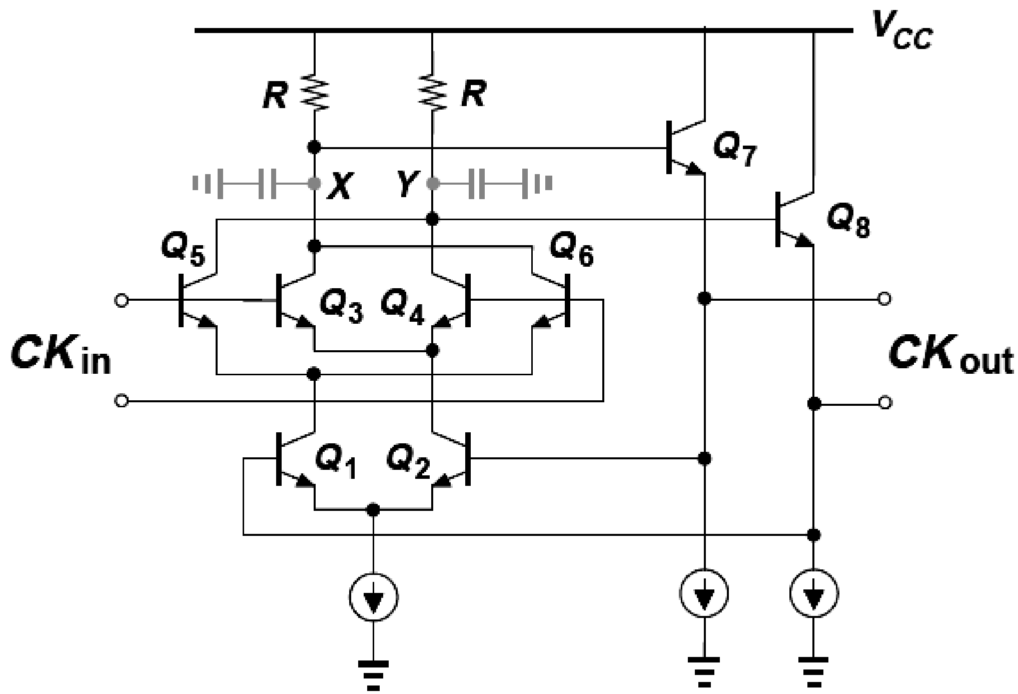


Dynamic (Miller) Divider



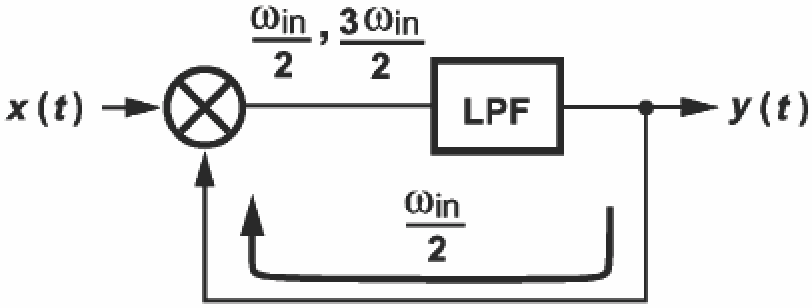
- Buffer input capacitance degrades the speed considerably.
- Speed limited to 18 GHz in 0.18−μm CMOS Technology.
- LPF absorbs circuit parasitics => High−speed operation.
- Circuit must satisfy certain phase shift requirements.

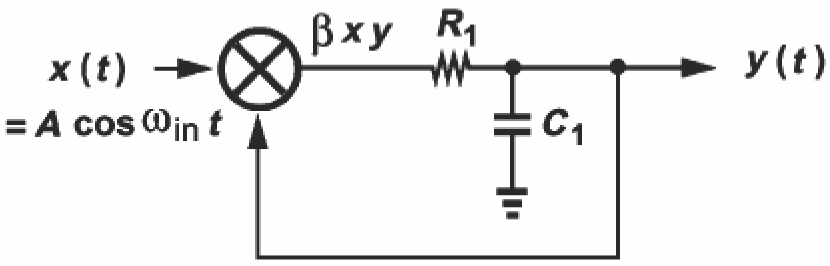
Conventional Dynamic Divider



- Exploits natural low−pass filtering at *X* and *Y*.
- Devices in the loop contribute enough phase shift for startup.
- But load resistance would consume large voltage headroom in CMOS.

Analysis of Dynamic (Miller) Divider





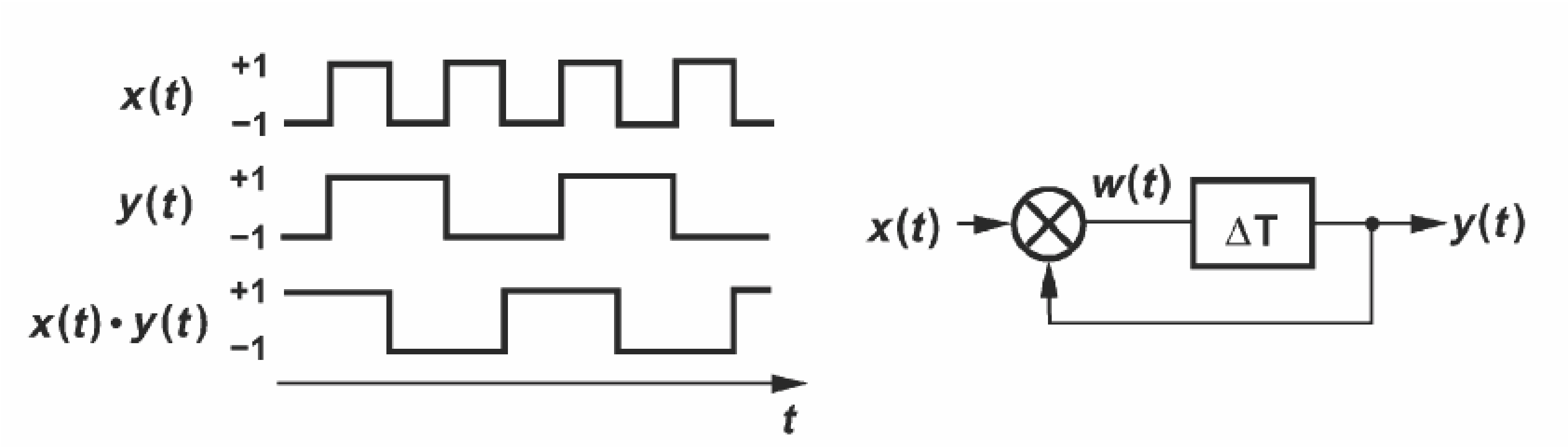
$$R_1C_1\frac{dy}{dt}+y=\beta yA\cos\omega_{in}t$$

⇨ $$y(t)=y(0)\exp\left(-\frac{t}{R_1C_1}+\frac{\beta A}{R_1C_1\omega_{in}}\sin\omega_{in}t\right)$$

⇨ **Decays to zero with a time constant of R_1C_1.**

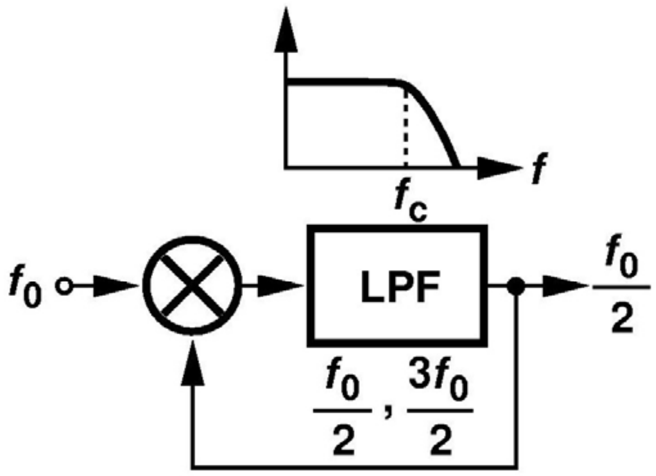
⇨ **Divider doesn't work without proper delay along the loop.**

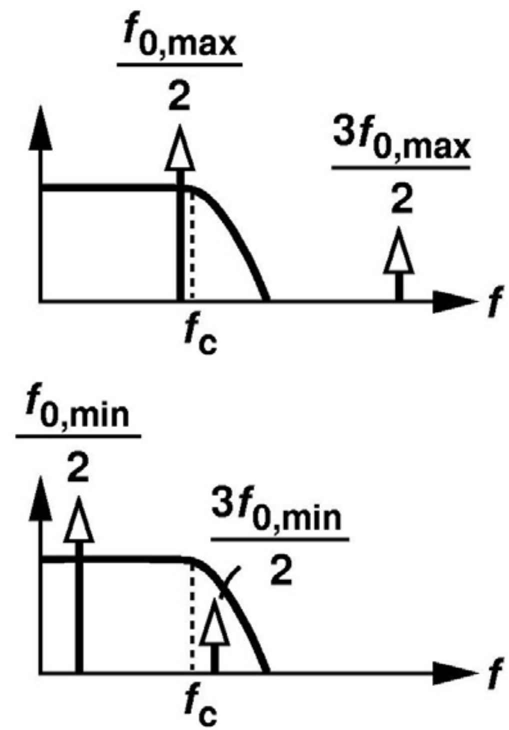
Analysis of Dynamic Divider



- 90° phase shift satisfies the division requirement.
- Usually an emitter follower is needed to provide the required phase shift.

Rough Estimation of Operation Range



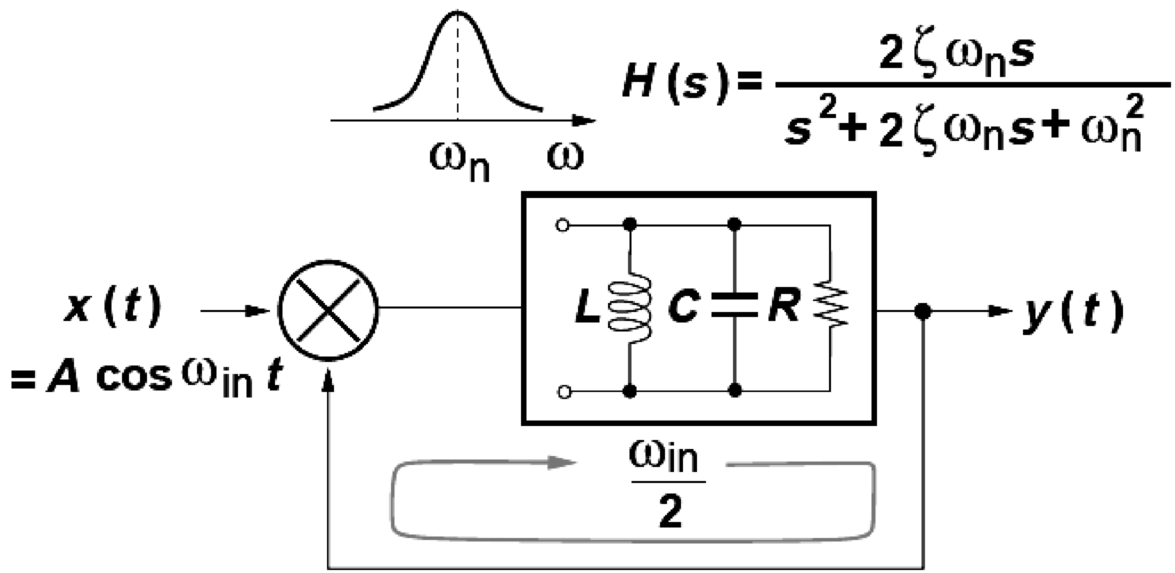


- The LPF must (1) filter out $\frac{3f_0}{2}$, (2) preserve $\frac{f_0}{2}$.

⇨ $\frac{f_{0,max}}{2} \cong f_c$ and $\frac{3f_{0,min}}{2} \cong f_c$

⇨ $\frac{2f_c}{3} < f_0 < 2f_c$

Dynamic Divider with Bandpass Load



Loop gain requirement:

$$\frac{\beta A}{2}\left|H\left(j\frac{\omega_{in}}{2}\right)\right| \geq 1$$

Thus,

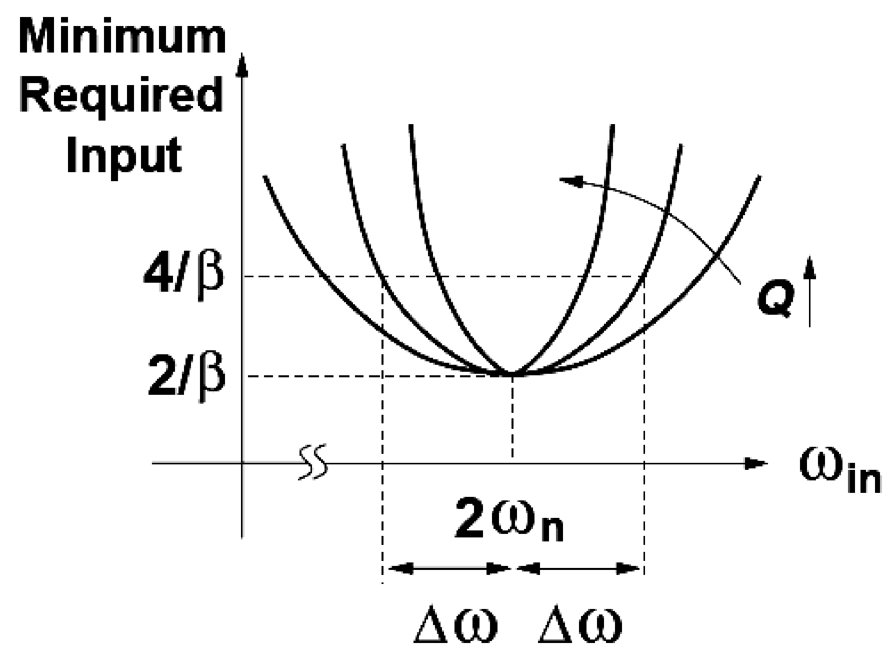
$$A \geq \frac{2}{\beta}\sqrt{1 + \frac{\left(1 - \frac{\omega_{in}^2}{4\omega_n^2}\right)^2}{\zeta^2 \frac{\omega_{in}^2}{\omega_n^2}}}$$

Frequency Range for Correct Division

$$A \geq \frac{2}{\beta}\sqrt{1+\frac{\left(1-\frac{\omega_{in}^2}{4\omega_n^2}\right)^2}{\zeta^2\frac{\omega_{in}^2}{\omega_n^2}}}$$

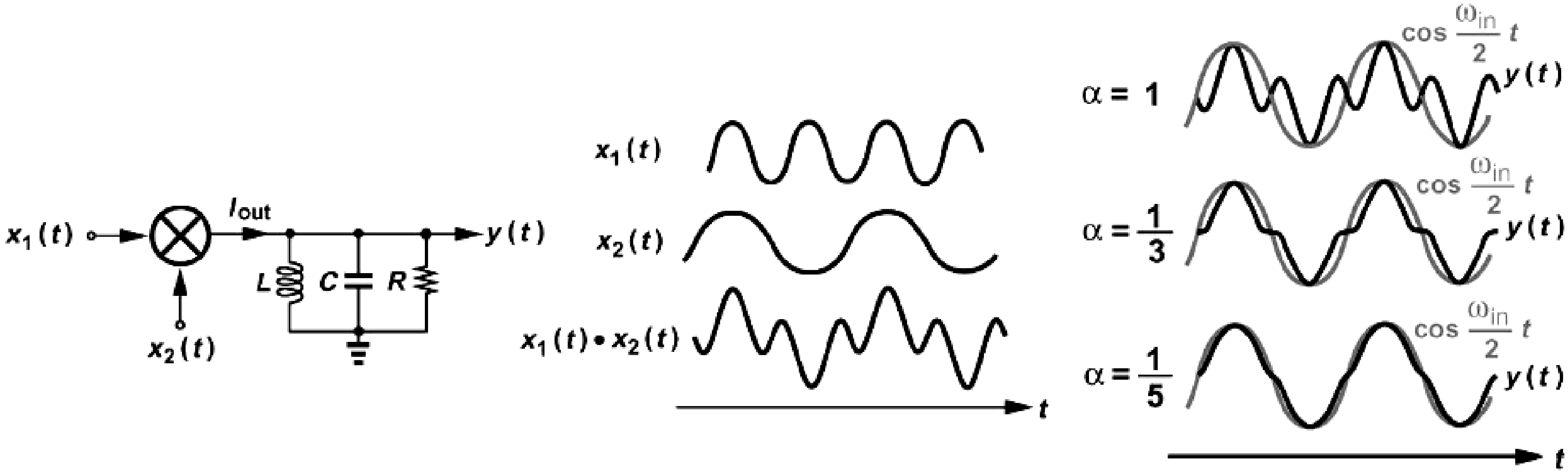
for $\Delta\omega = |\omega_{in} - 2\omega_n| << 2\omega_n$:

$$A \geq \frac{2}{\beta}\sqrt{1+\left(\frac{Q\,\Delta\omega}{\omega_n}\right)^2}$$



For Example, if $A_{max} = \frac{4}{\beta}$, $\Delta\omega = \frac{\sqrt{3}}{Q}\omega_n$

Intuitive Understanding of Bandpass Division

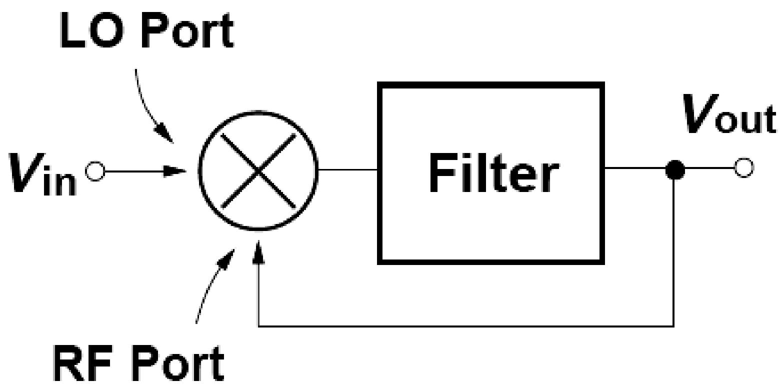


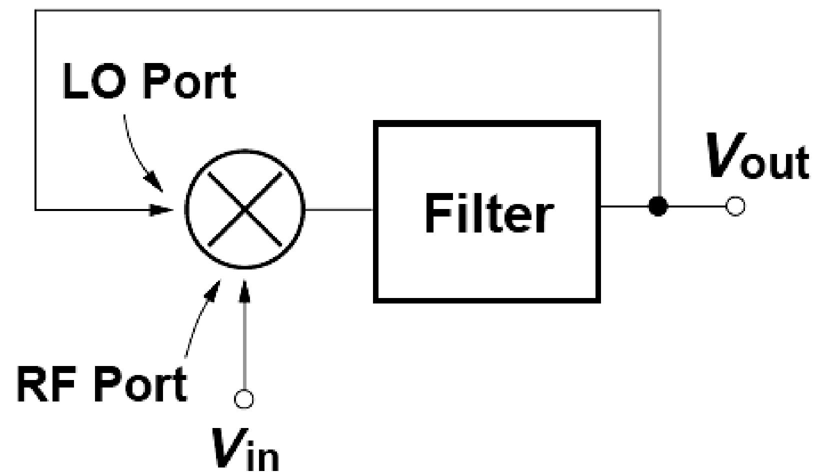
$$y \propto \cos\frac{\omega_{in}t}{2} + \alpha\cos\frac{3\omega_{in}t}{2} \quad \Rightarrow 0 < \alpha < 1/3.$$

Actually, $\Rightarrow 0 < \alpha < 1/(2\sqrt{3})$**.**

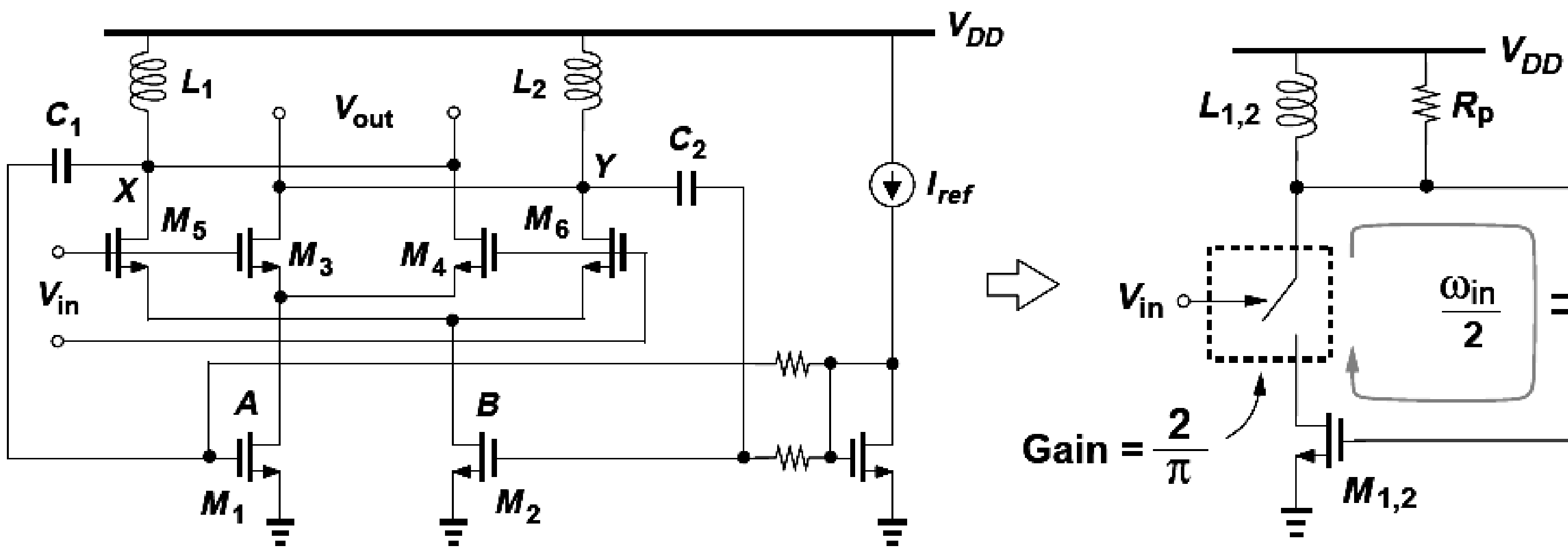
Reference: "A 40-GHz Frequency Divider in 0.18-um CMOS Technology", JSSC, April 2004.

RF-Port and LO-Port Feedback





RF-Port Feedback



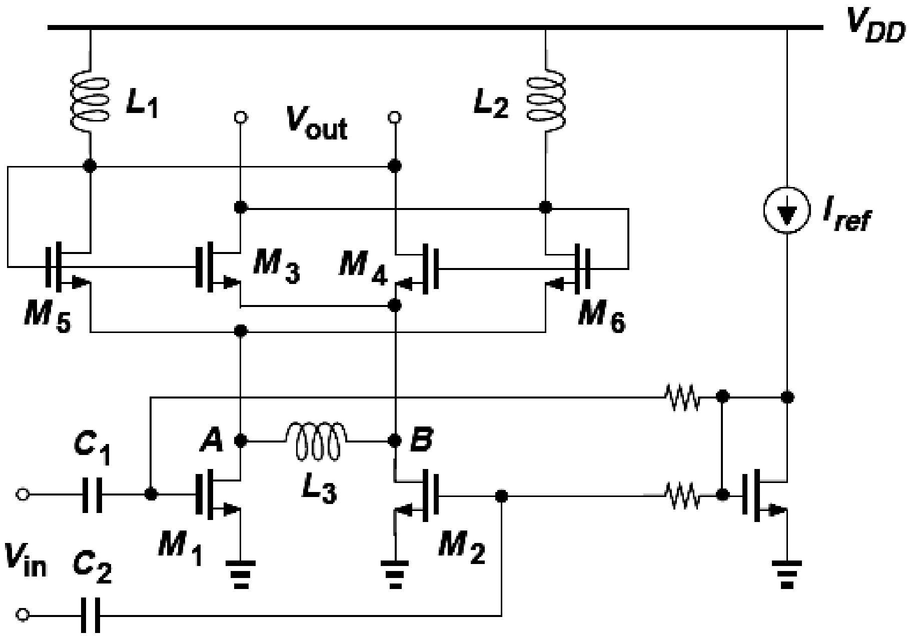
Nonidealities:

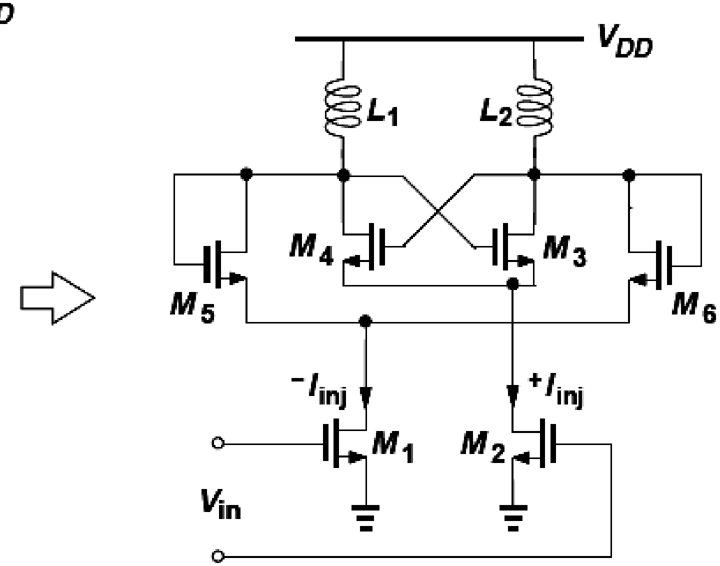
- Current Loss at A and B
- Gradual Switching of M_3-M_6
- Parasitics at X and Y

Loop gain $= \frac{2}{\pi} g_{m1,2} R_p$

$$\begin{cases} R_p = Q L_{1,2} \dfrac{\omega_{in}}{2} \\ g_m = 2\pi f_T C_{GS} \\ \dfrac{\omega_{in}}{2} = \dfrac{3}{\sqrt{C_{GS} L_{1,2}}} \end{cases} \Rightarrow \quad Q = \frac{\pi}{2} \cdot \frac{f_{in}/2}{f_T}$$

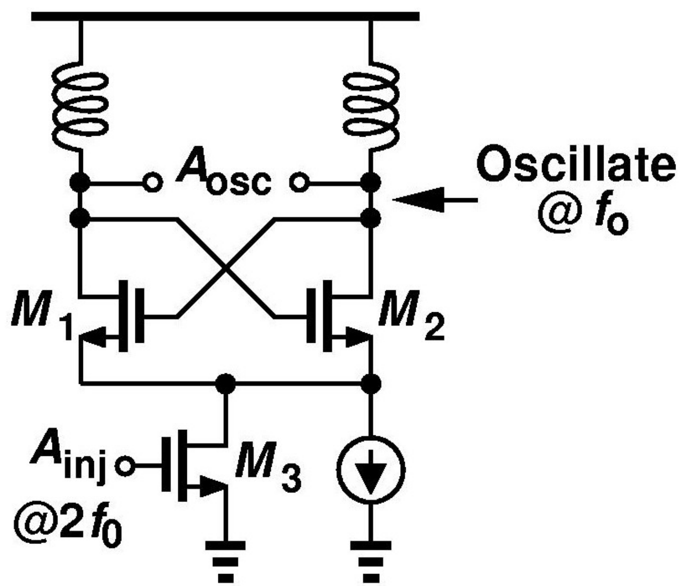
LO-Port Feedback

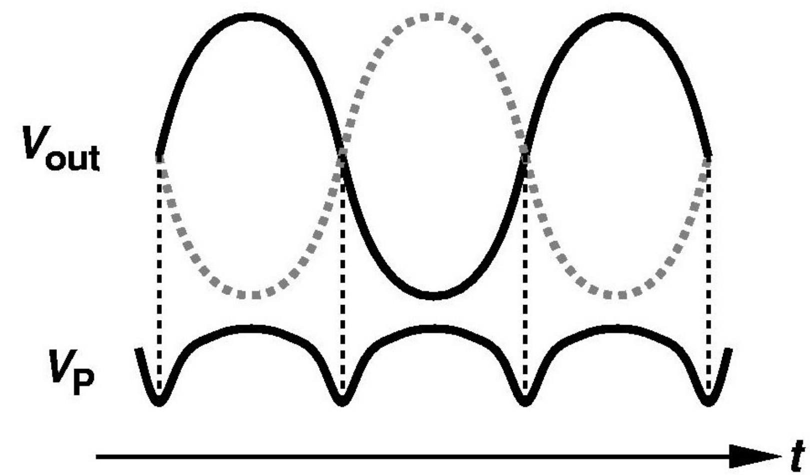




- With feedback applied to LO port, the circuit resembles an injection−locked divider.

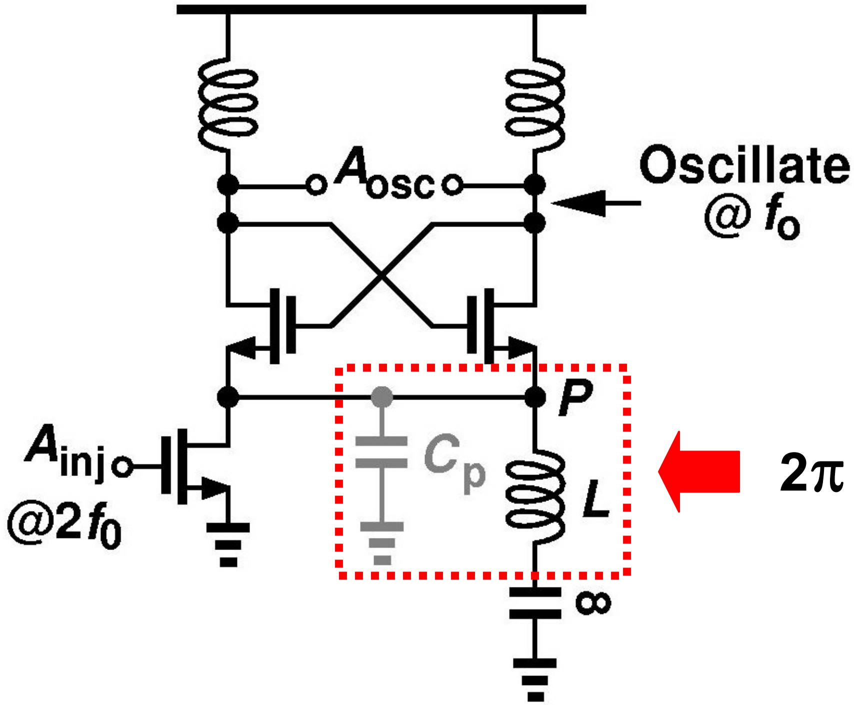
Injection-Locked Divider





- Injecting signal at twice the oscillation frequency.
- Locking range $\cong \dfrac{f_0}{2Q} \cdot \dfrac{A_{inj}}{A_{osc}} \cdot \dfrac{4}{3\pi}$

Modified Injection-Locked Divider

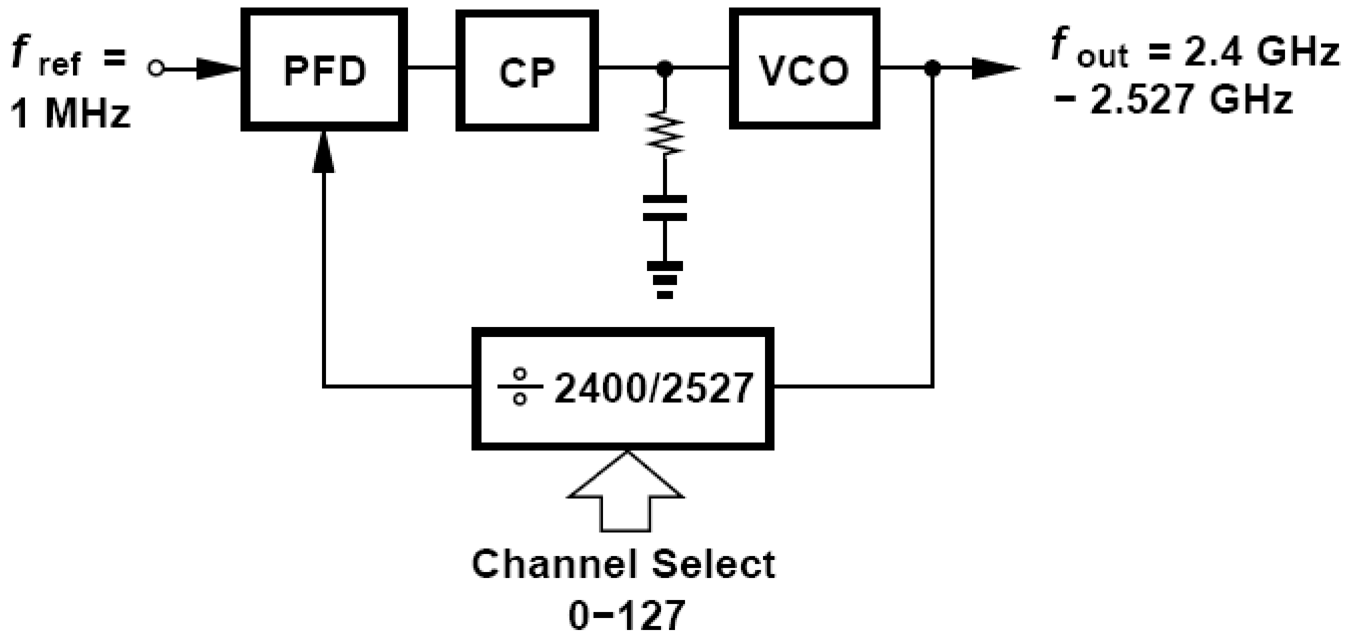


$$2\pi \cdot 2f_0 = \frac{1}{\sqrt{LC_P}}$$

- Resonate out parasitic capacitance at node *P* to allow stronger signal injection to the divider.

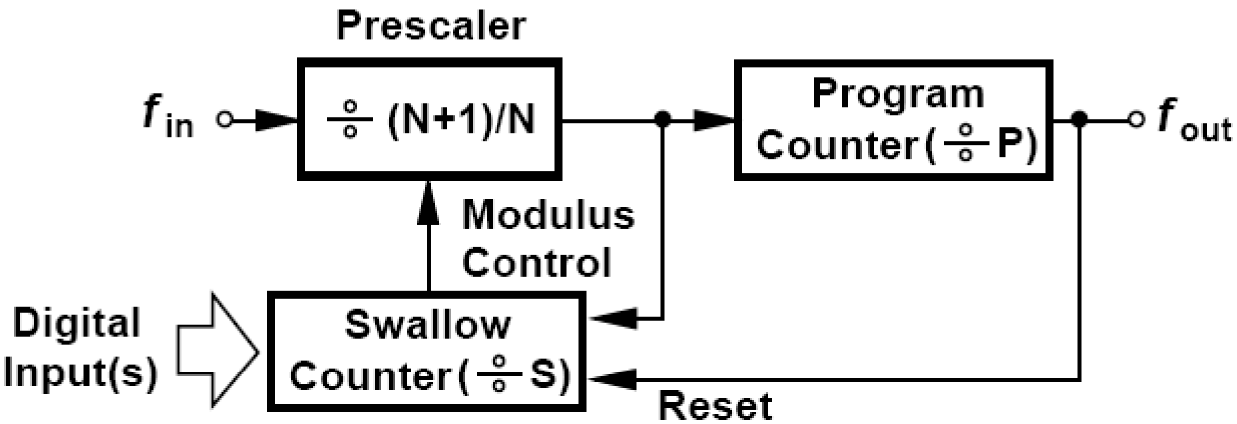
Multi-Modulus Divider

- Some applications require programmable division.
- Example: Integer-N Frequency Synthesizer.



Channel Spacing = 1 MHz, Channel Number = 128

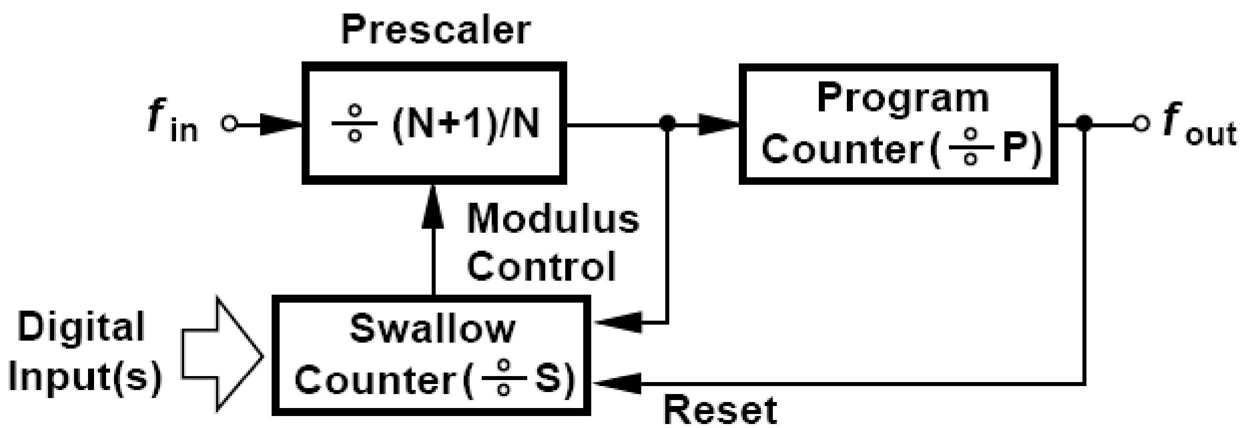
Pulse-Swallow Divider



$$f_{out} = \frac{f_{in}}{NP+S}$$

- Prescaler divides the input frequency by N$+$1 or N based on the modulus control.
- Program counter divides the prescaler output by P (fixed).
- Swallow counter divides the prescaler output by S (programmable).

Pulse-Swallow Divider



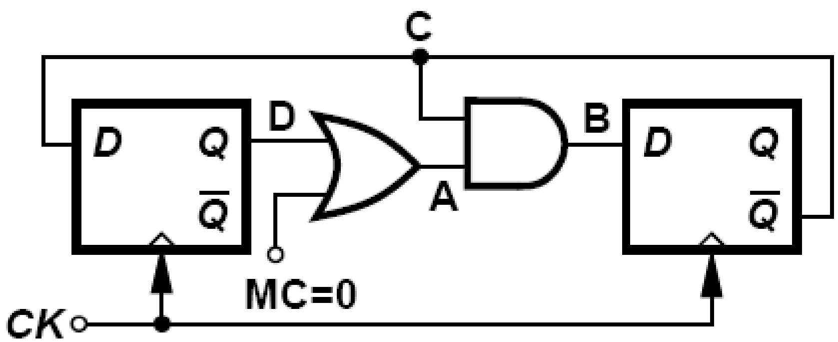
$$f_{out} = \frac{f_{in}}{NP+S}$$

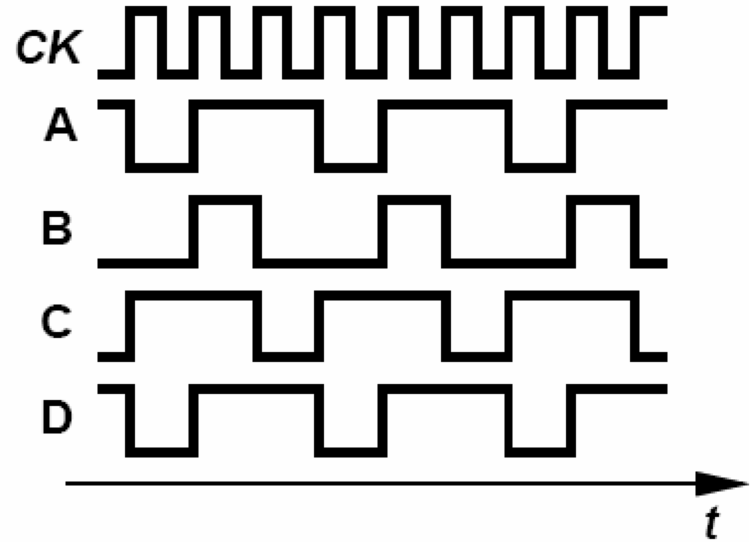
- Start from reset, prescaler divides by $N+1$ until swallow counter is full.
- After $(N+1)S$ pulses at the input, the modulus control changes to N.
- Continues to count until program counter is full.

$\Rightarrow$ Total pulses at the input = $(N+1)S+N(P-S)$ = $NP+S$.

Prescaler (Dual-Modulus Dividers)

- ÷3/2 Divider

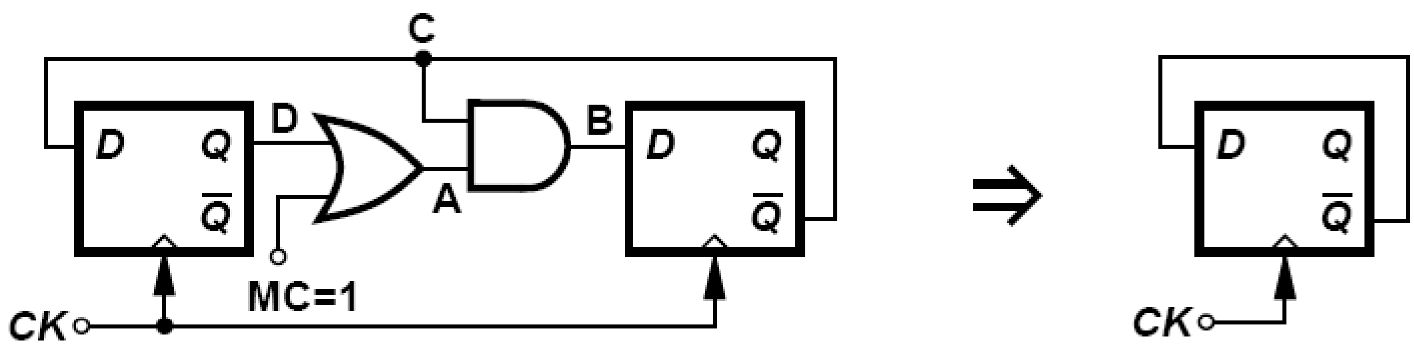




- When MC=0 ⇒ OR Gate transparent ⇒ ÷3

Prescaler (Dual-Modulus Dividers)

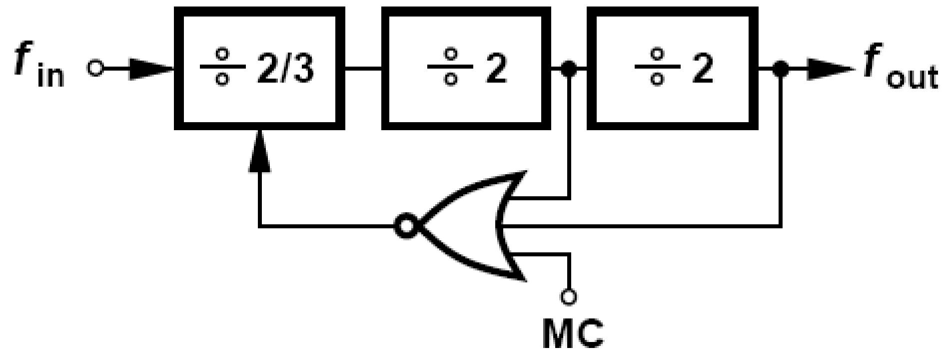
❐ ÷3/2 Divider



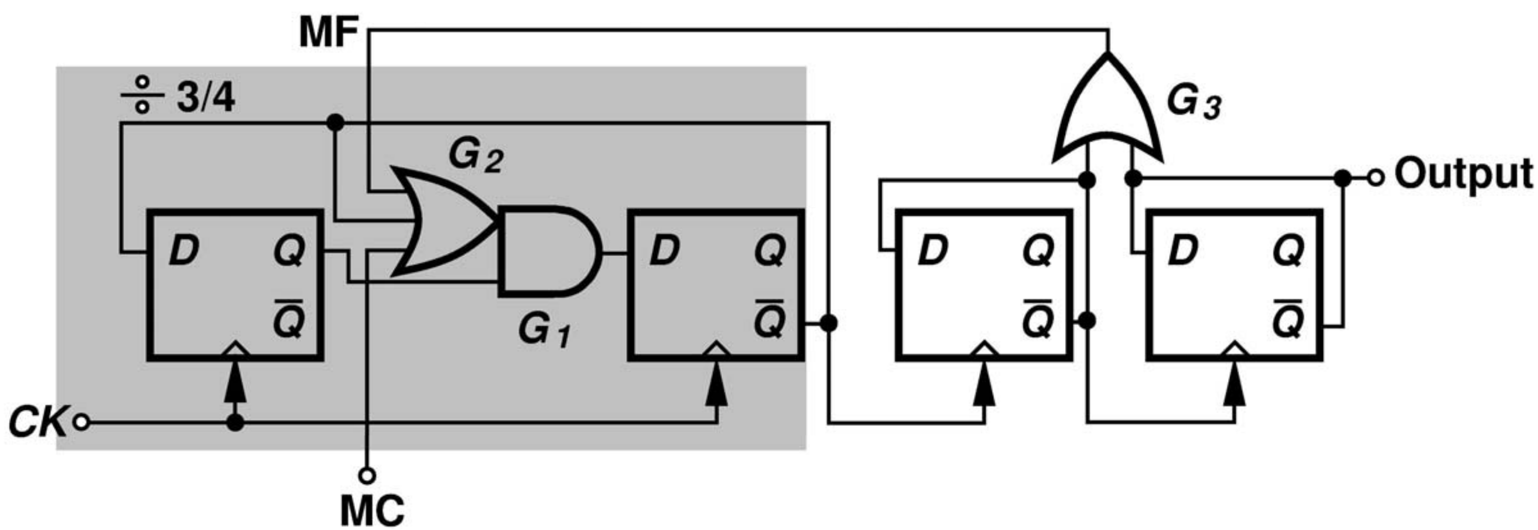
❐ When MC=1 ⇒ A=1, B=C ⇒ degenerates to ÷2 circuit

Higher Modulus Prescaler

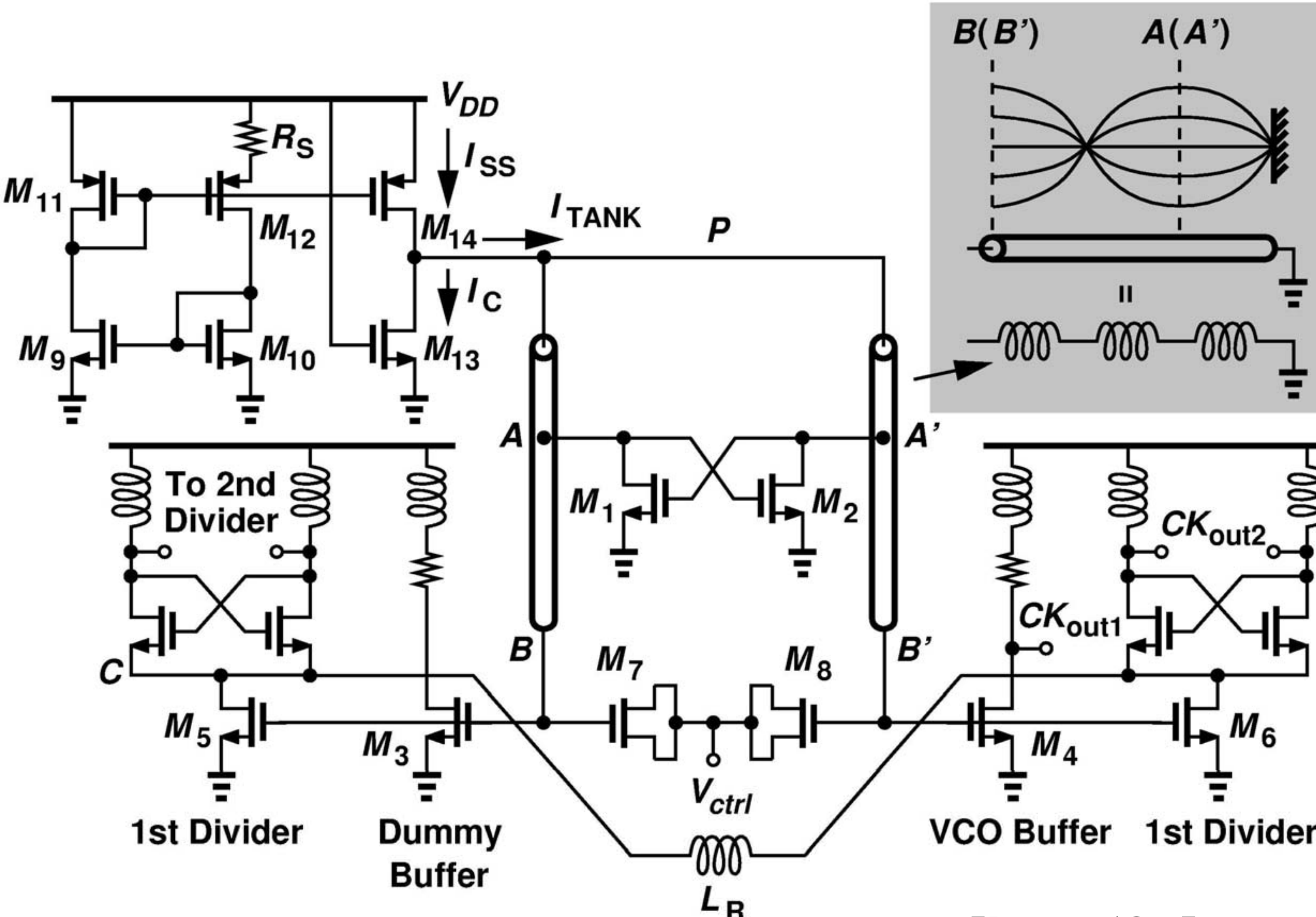
- ÷8/9 Divider



- ÷15/16 Divider



Case Study

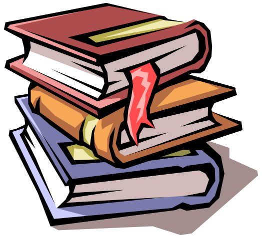


[Lee, '07]

Mixers, Multiplexers, and Demultiplexers

Professor Jri Lee

台大電子所　李致毅教授



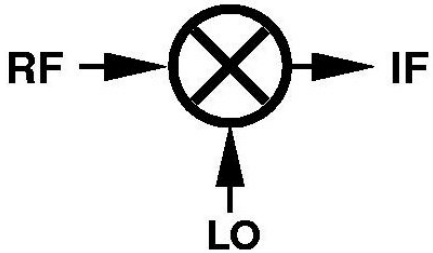
Electrical Engineering Department

National Taiwan University

Outline

- Mixers
  - Passive and Active
  - Bipolar and CMOS
- Muxes
  - 2-to-1
  - N-to-1
- Demuxes
- Case Study

Performance Metrics of Mixers



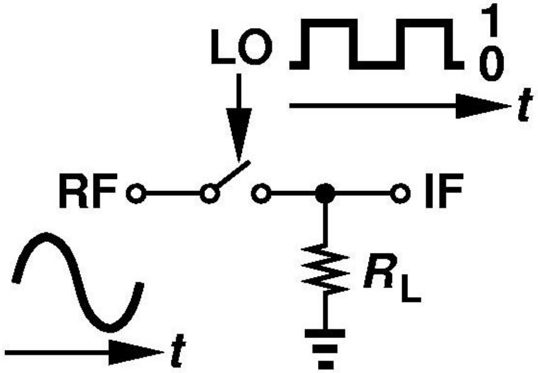
NF	8-12 dB
IIP3	0-5 dBm
R_{in}	50 Ω (Standalone)
Gain	10-15 dB
LO-RF Isolation	
LO-IF Isolation	

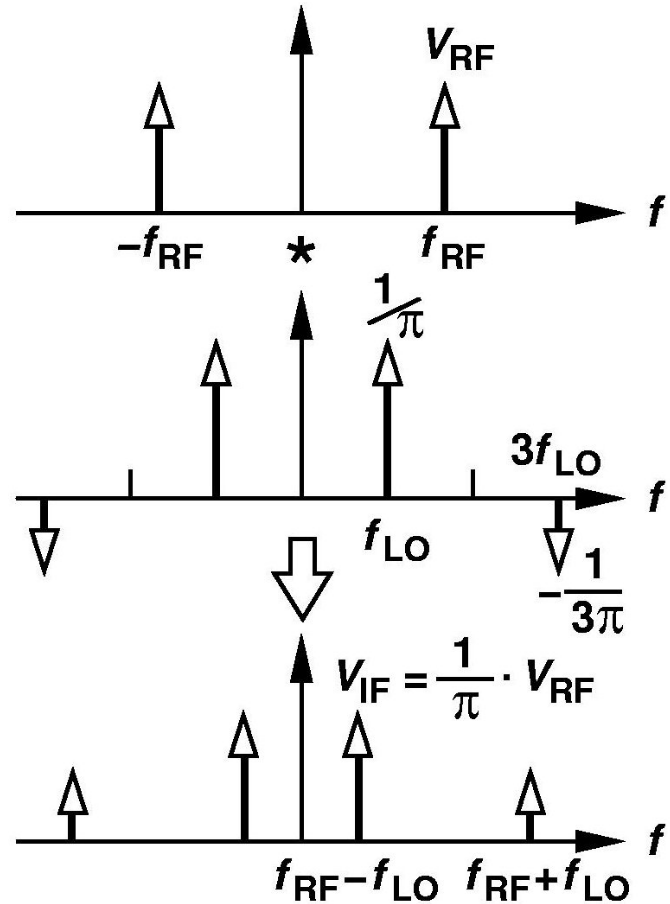
- **Voltage and Power Conversion Gains:**

$$A_V = \frac{V_{IF}}{V_{RF}} \qquad A_P = \frac{P_{IF}}{P_{RF}}$$

- **A_V and A_P need not to be equal because the source and load impedances are different.**

Passive Mixers





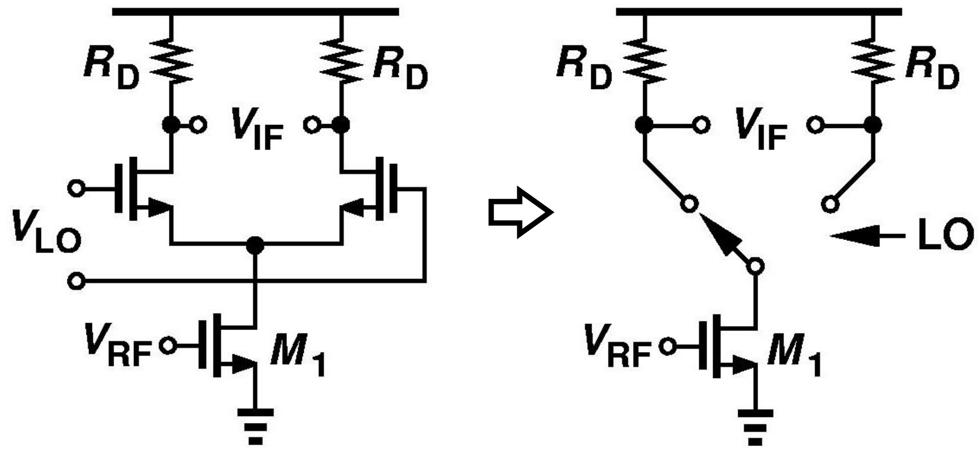
***LO signal with 50% duty cycle**

$$V_{IF} = V_{RF} \cdot S(t)$$

- **Voltage conversion gain = $1/\pi \approx -6.4$ dB**
- **Tradeoff: sinusoidal LO (no higher-order harmonics) vs. squarewave LO (abrupt transition)**

Active Mixers

- Differential realization

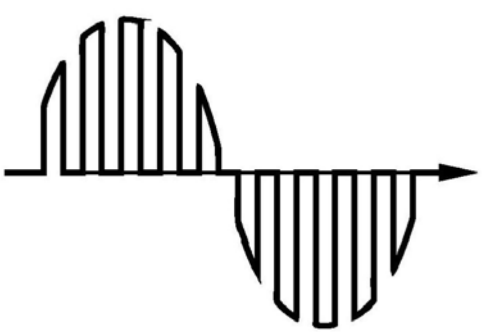


$$V_{IF} = g_{m1} \cdot V_{RF} \cdot R_D \cdot \frac{2}{\pi}$$

⇨ Voltage conversion

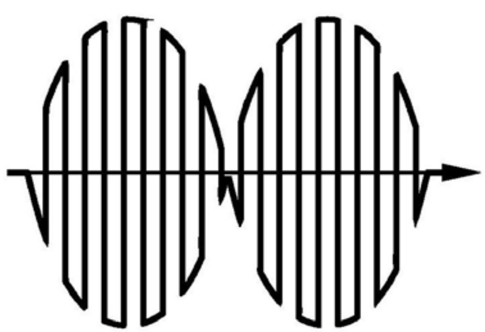
$$\text{gain} = g_{m1} \cdot R_D \cdot \frac{2}{\pi}$$

Single-Ended



Conv. gain = $\frac{1}{\pi}$

Differential

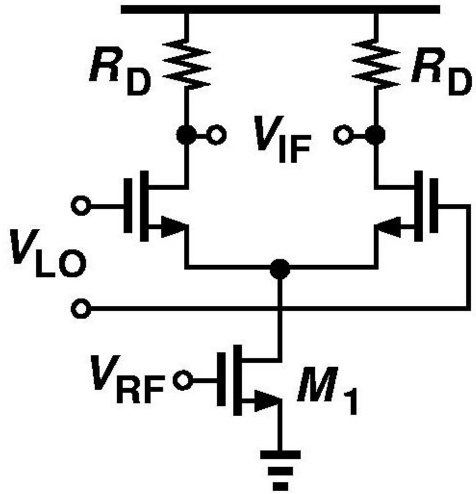


Conv. gain = $\frac{2}{\pi}$

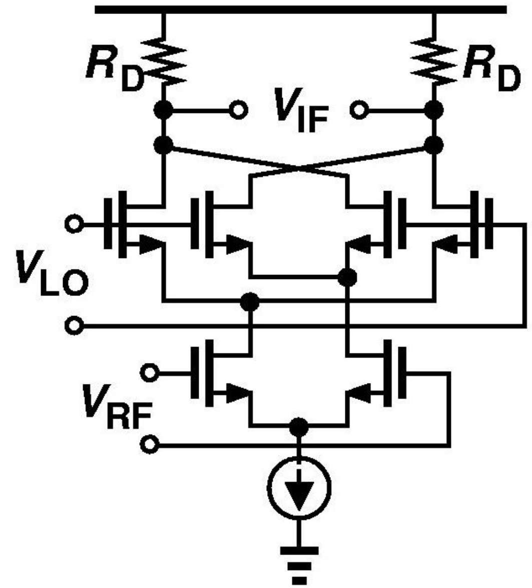
- LO signal couples to IF.
- Gradual LO ⇒ RF signal appears as common-mode ⇒ reduce conversion gain.

Single-Balance and Double-Balance Mixers

- Single-Balanced

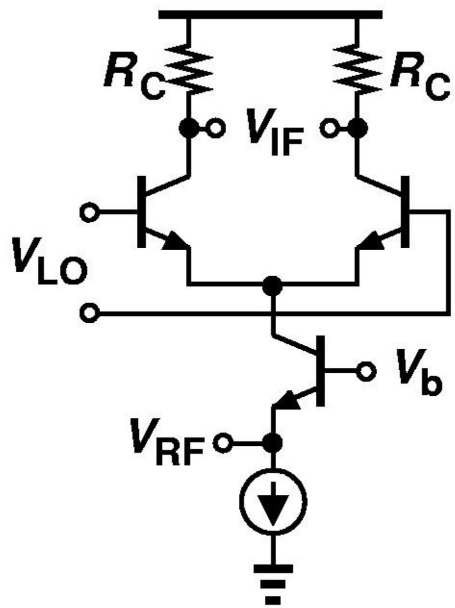


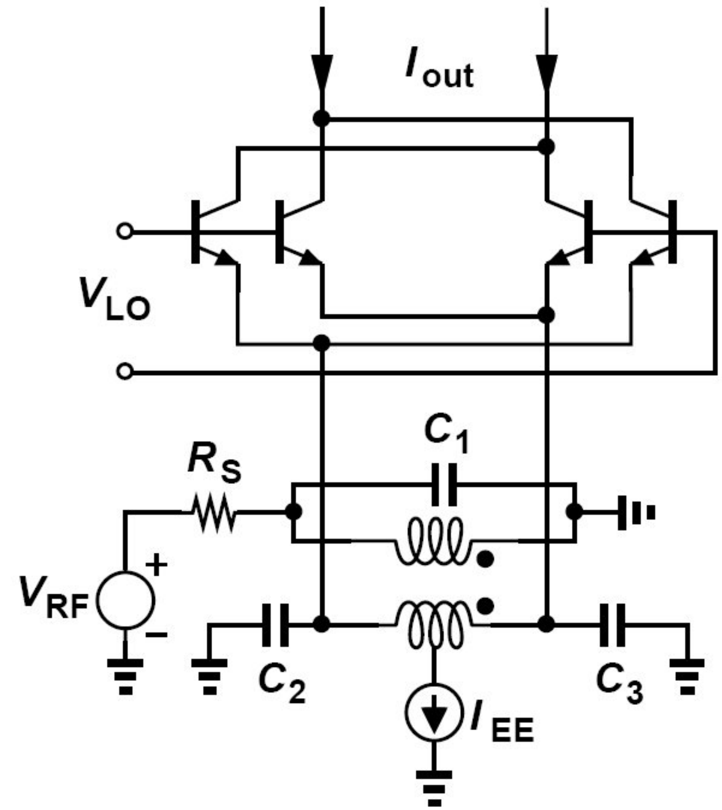
- Double-Balanced



	Single	Double
Noise	Lower	Higher
LO-IF Feedthrough	Higher	Lower
Even-Order Distortion	Higher	Lower
Conversion Gain	Lower	Higher(2x)

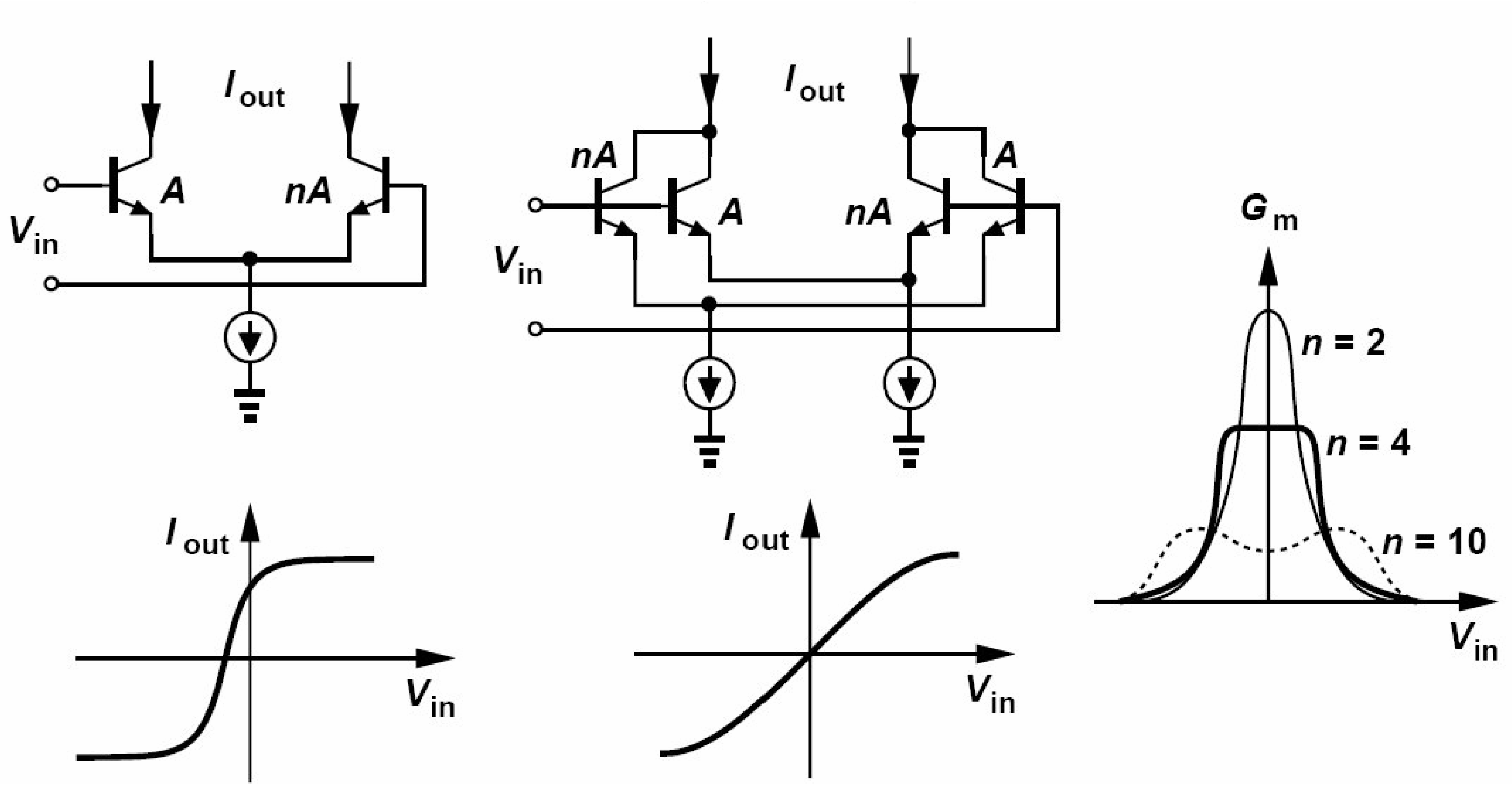
Bipolar Mixers





- $A_V = g_{m1} \cdot R_C \cdot \frac{2}{\pi}$
- Linearity
- Power Consumption
- LO-IF Feedthrough
- LO-RF Feedthrough
- Incorporating single-ended/ differential conversion.

Linearization Technique

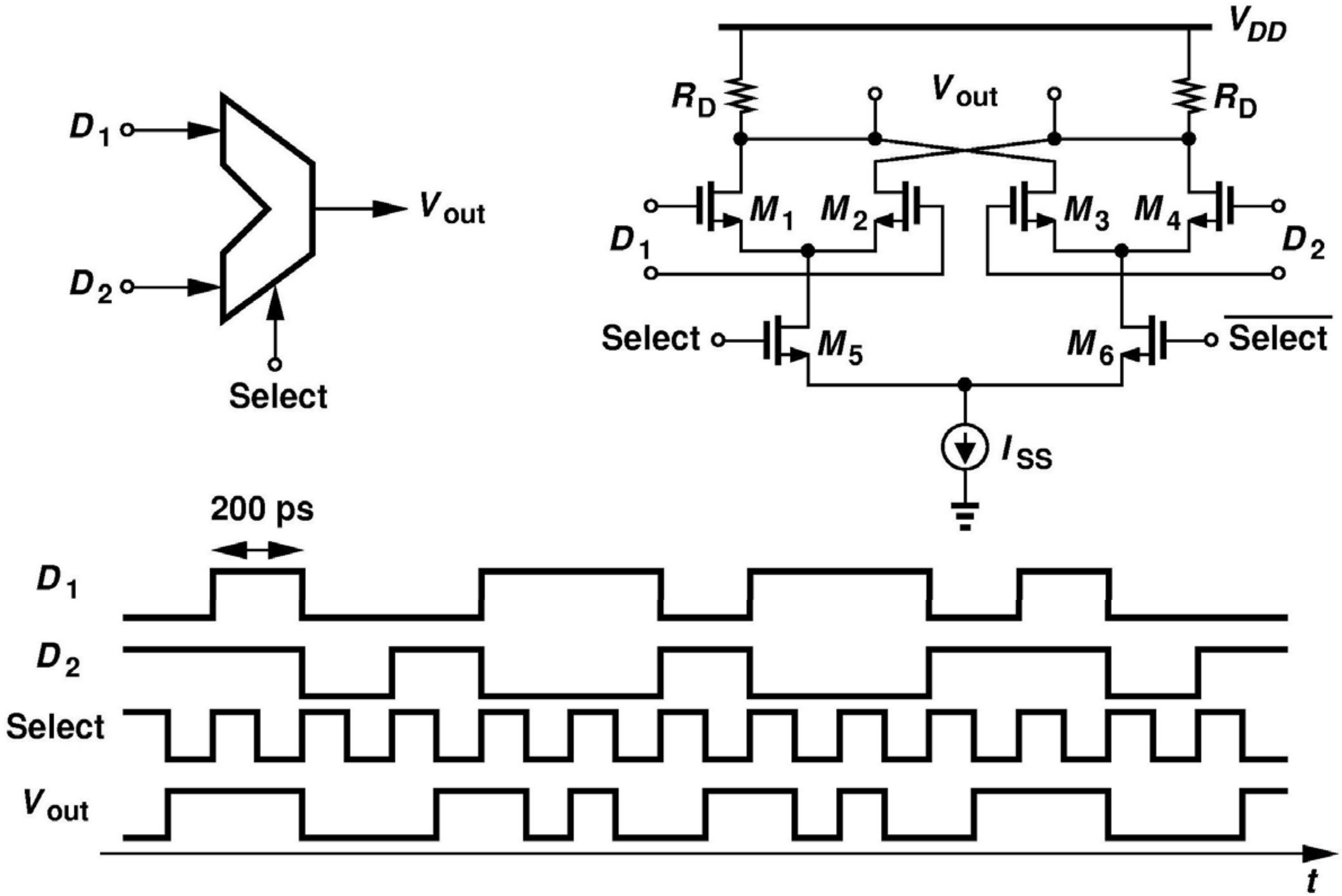


- Does *n* matters if constant G_m is of importance?

CMOS Mixers

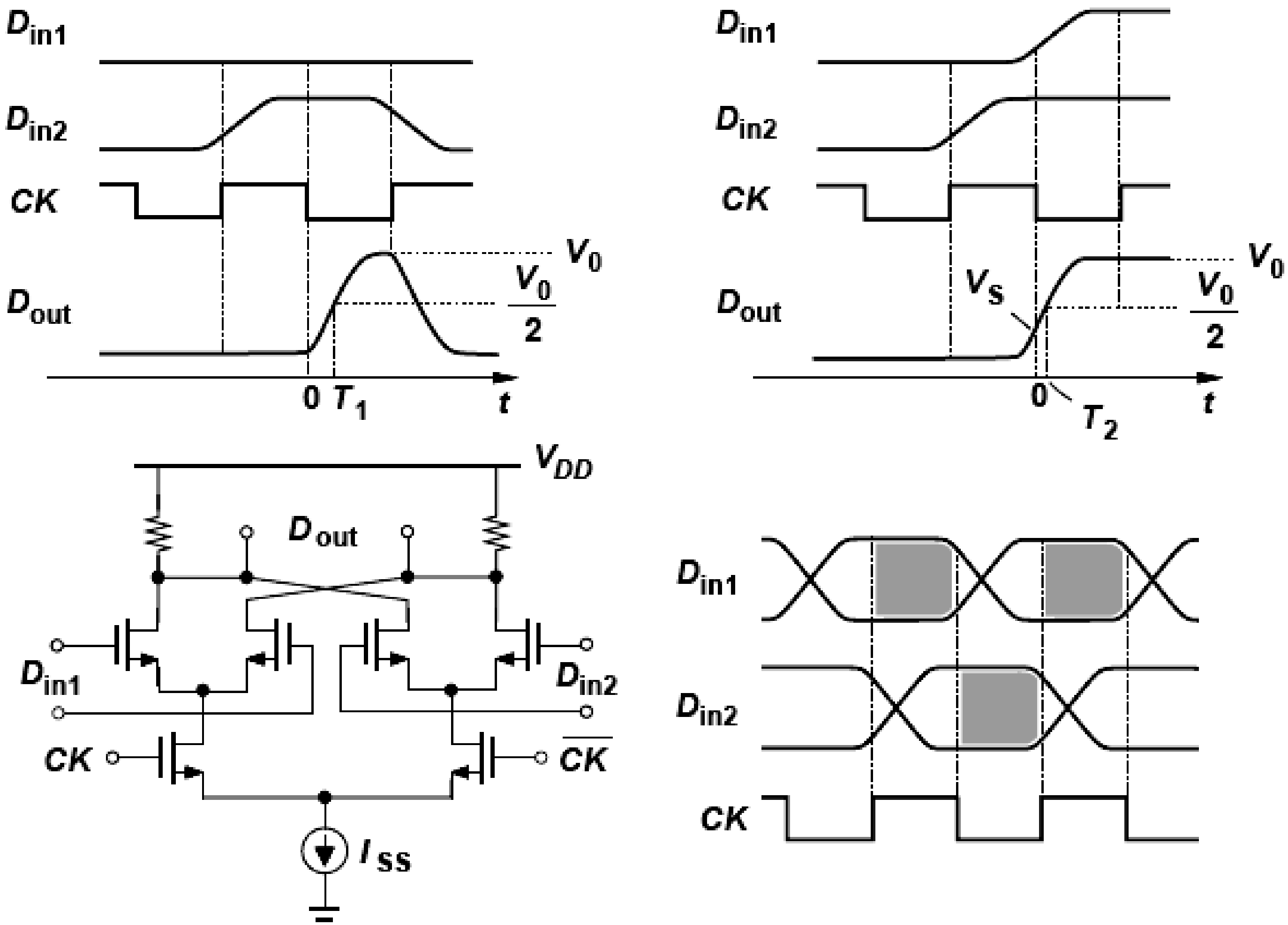
- **Most of the bipolar design concepts can be applied to CMOS directly, $\Rightarrow$ only LO requirement differs.**
- **Small LO signal $\Rightarrow$ lower conversion gain, higher noise, higher nonlinearity.**
- **To make the switching sharp for a given LO $\Rightarrow$ increase the width of the differential pair or reduce the bias current $\Rightarrow$ lower speed or lower gain.**

2-to-1 Selector



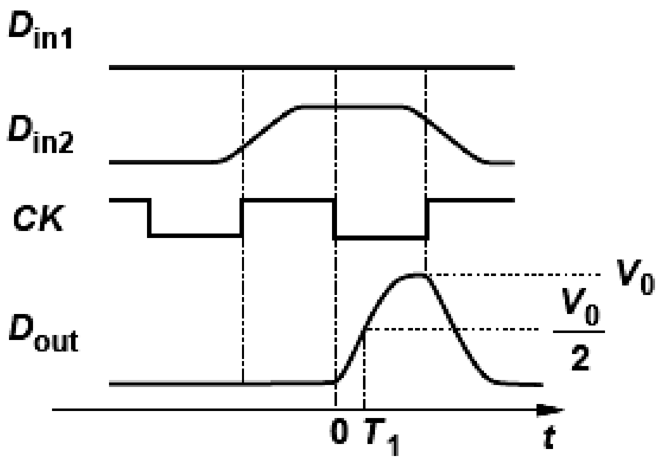
- Finite rising and falling edges ⇒ timing issues

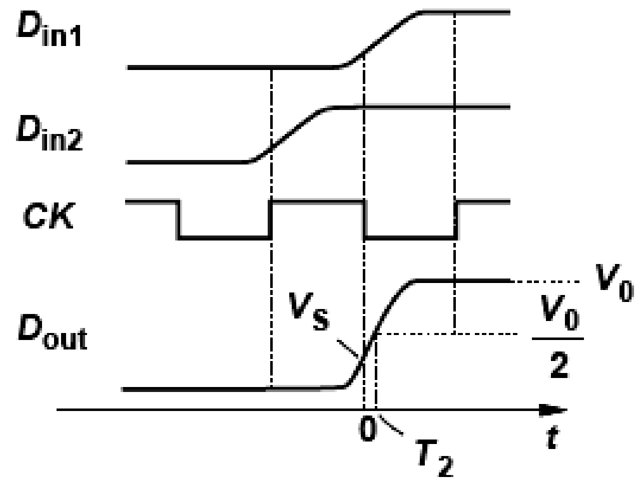
Deterministic Jitter of MUX



- Imperfect alignment along with finite transition time of inputs cause deterministic jitter.

Deterministic Jitter of MUX

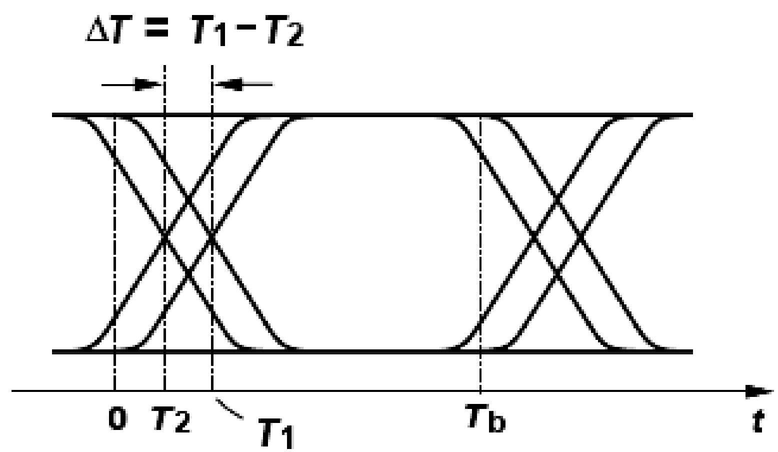




$$T_1 = \tau \ln 2$$

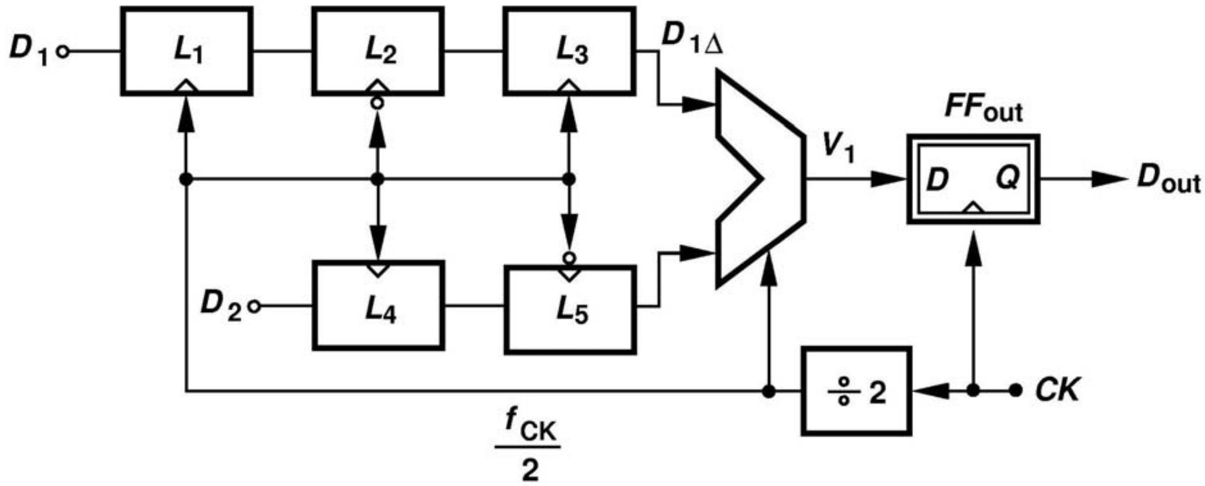
$$T_2 = \tau\left[\ln(V_0 - V_S) - \ln\frac{V_0}{2}\right]$$

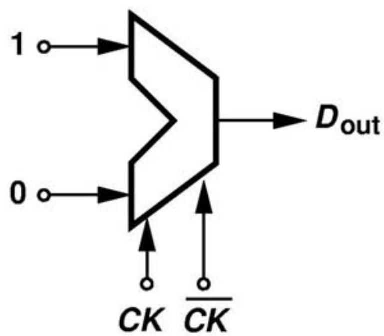
$$\frac{\Delta T}{T_b} = \frac{T_1 - T_2}{T_b} = \frac{\ln\left(\frac{V_0}{V_0 - V_S}\right)}{2\pi}$$

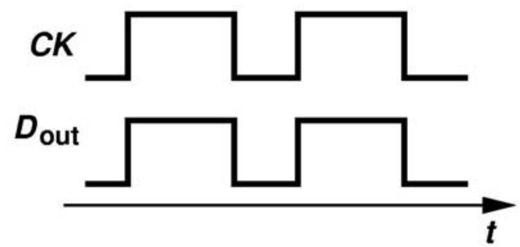


- For $V_s = \frac{V_0}{4}$, $\frac{\Delta T}{T_b} = 4.6\%$

Output Data Cleanup with Flipflop

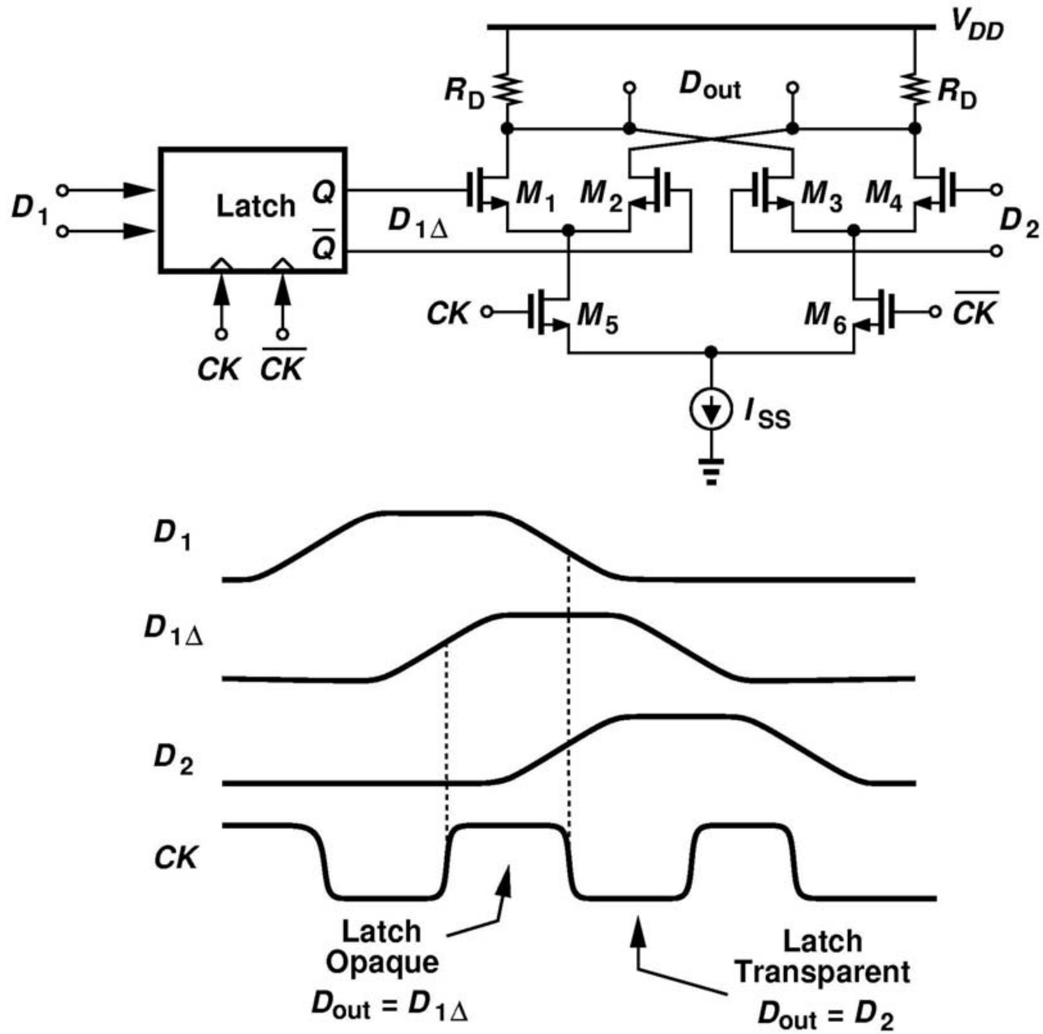






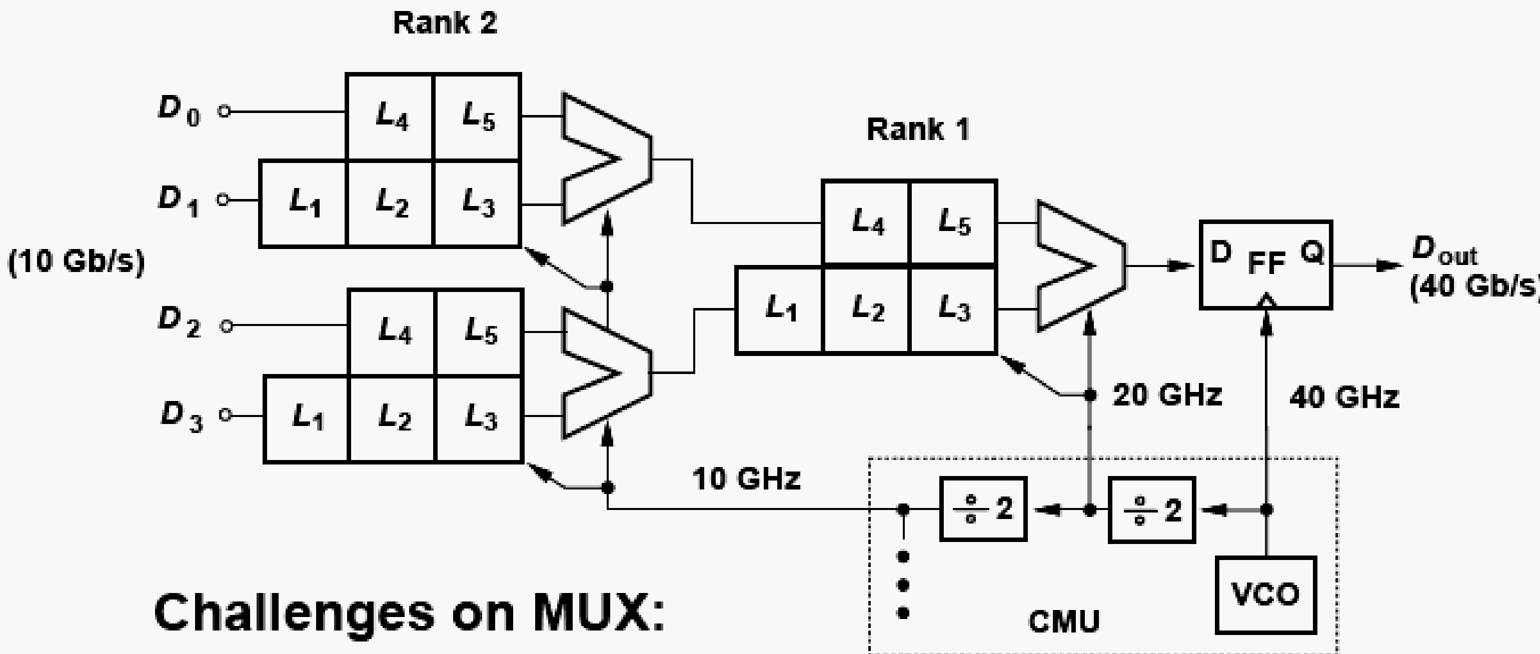
- Data skew and clock imbalance would cause output distortion directly.
- A full-rate FF can remedy this.

Sampling Alignment Using Latches



- Usually requires latches to provide 0.5 UI phase shift.

N-to-1 Multiplexer with Tree Structure

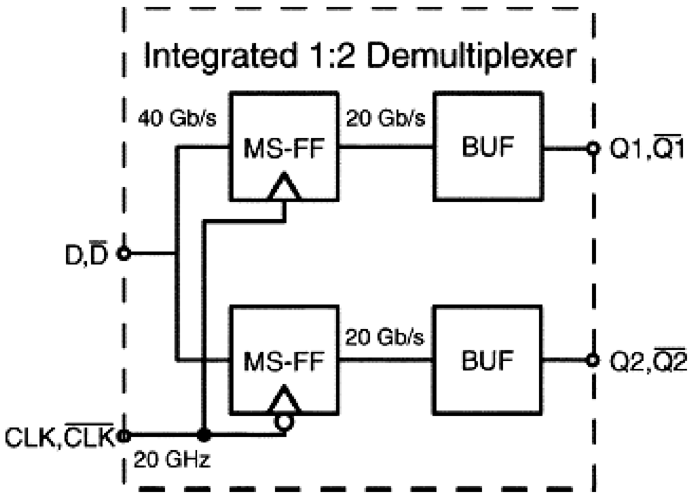


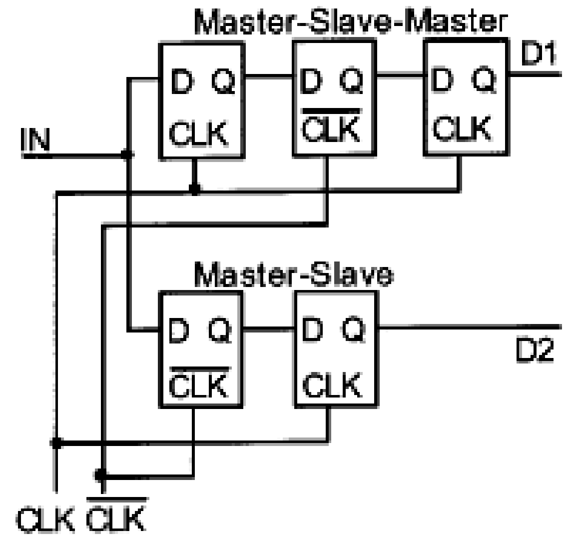
Challenges on MUX:

- ❐ Data Alignment
- ❐ Finite Transition Time
- ❐ Broadband Operation
- ❐ Power Dissipation

⇒ **and also, clock distribution.**

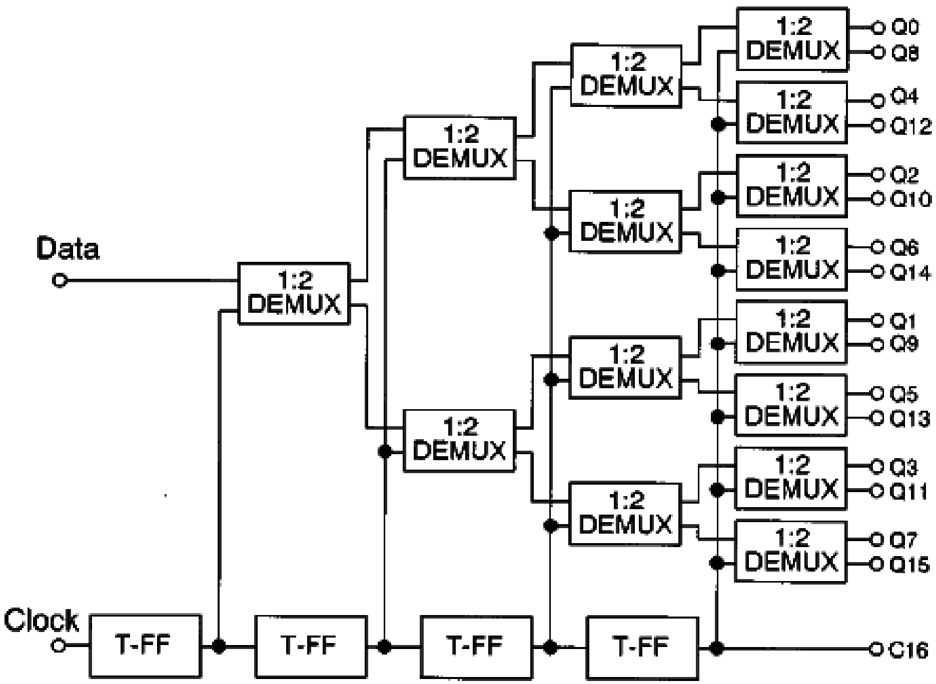
Demultiplexer

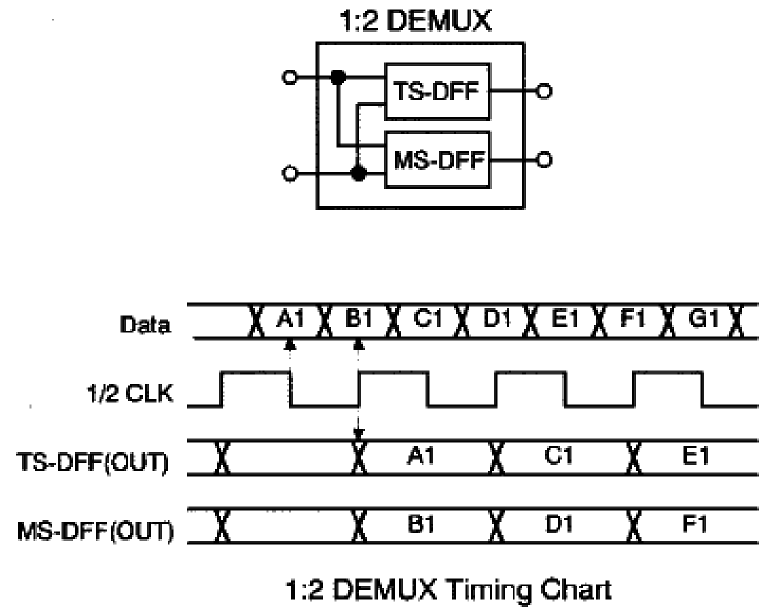




- Reverse operation of MUX.
- Much more relaxed clock/data phase requirement.
- Usually work with CDR.

Case Study (I)

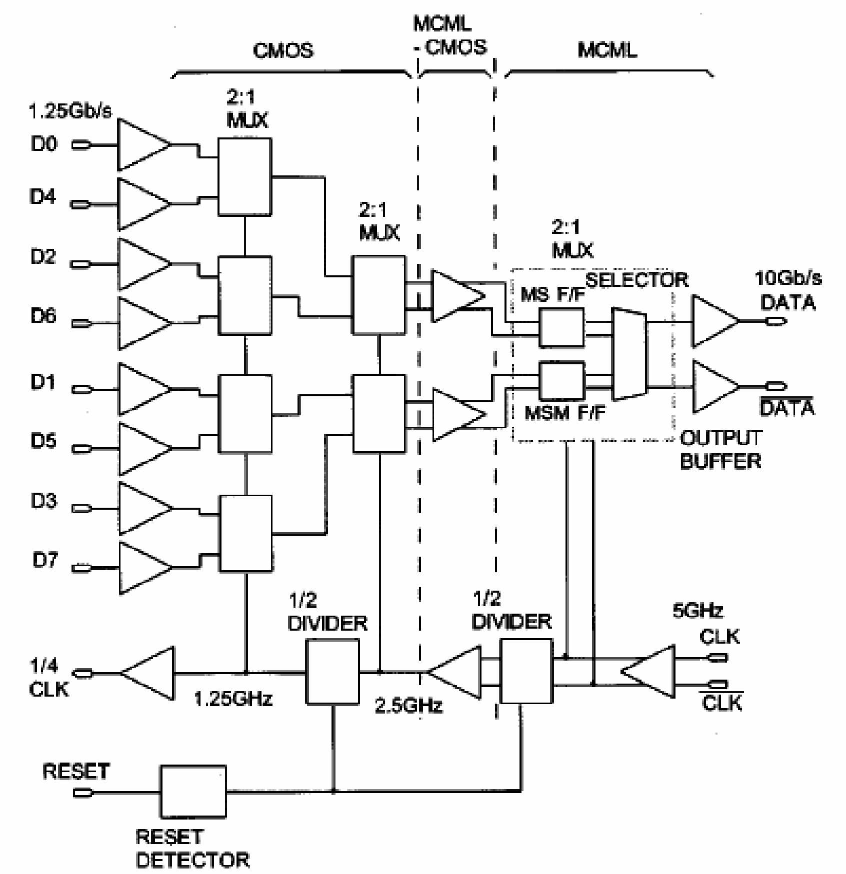


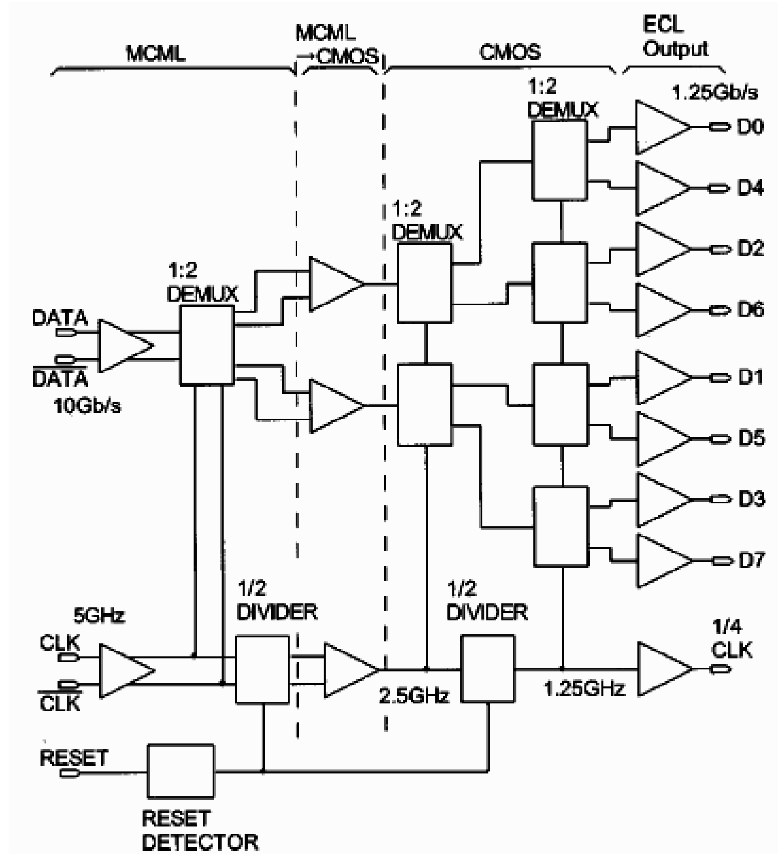


[Ishii, JSSC02]

- ❒ Tree structure.
- ❒ InP technology.
- ❒ Timing requirement relaxes as speed goes down.

Case Study (II)





[Tanabe, JSSC’01]

Phase-Locked Loops

Professor Jri Lee

台大電子所　李致毅教授

Electrical Engineering Department
National Taiwan University

Outline

- Introduction
- Simple PLLs
- Charge-Pump PLLs
- Nonidealities
- Applications

Phase-Locked Loops and their Versatileness

- Phase-locking technique provides an unique ability in phase/frequency acquisition, creating numerous important applications in electronics, communication, and instrumentation.

- Playing indispensable roles in communications and computation systems.

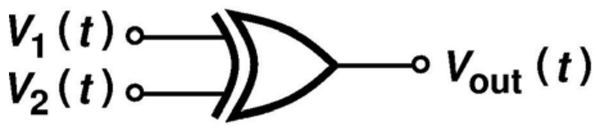
- Examples:

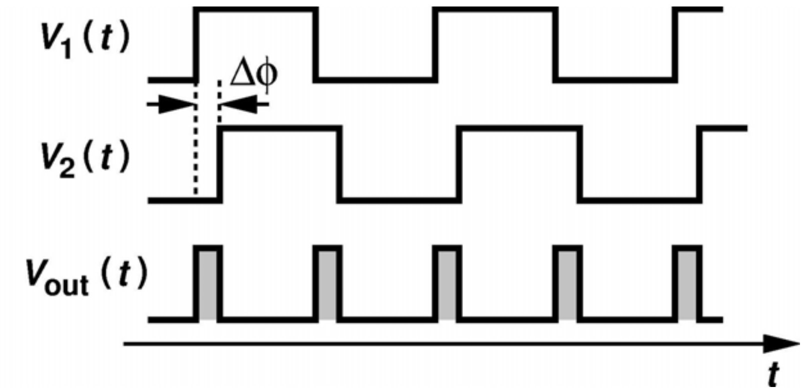
  Frequency synthesis

  Clock and data recovery

  Clock generation and distribution

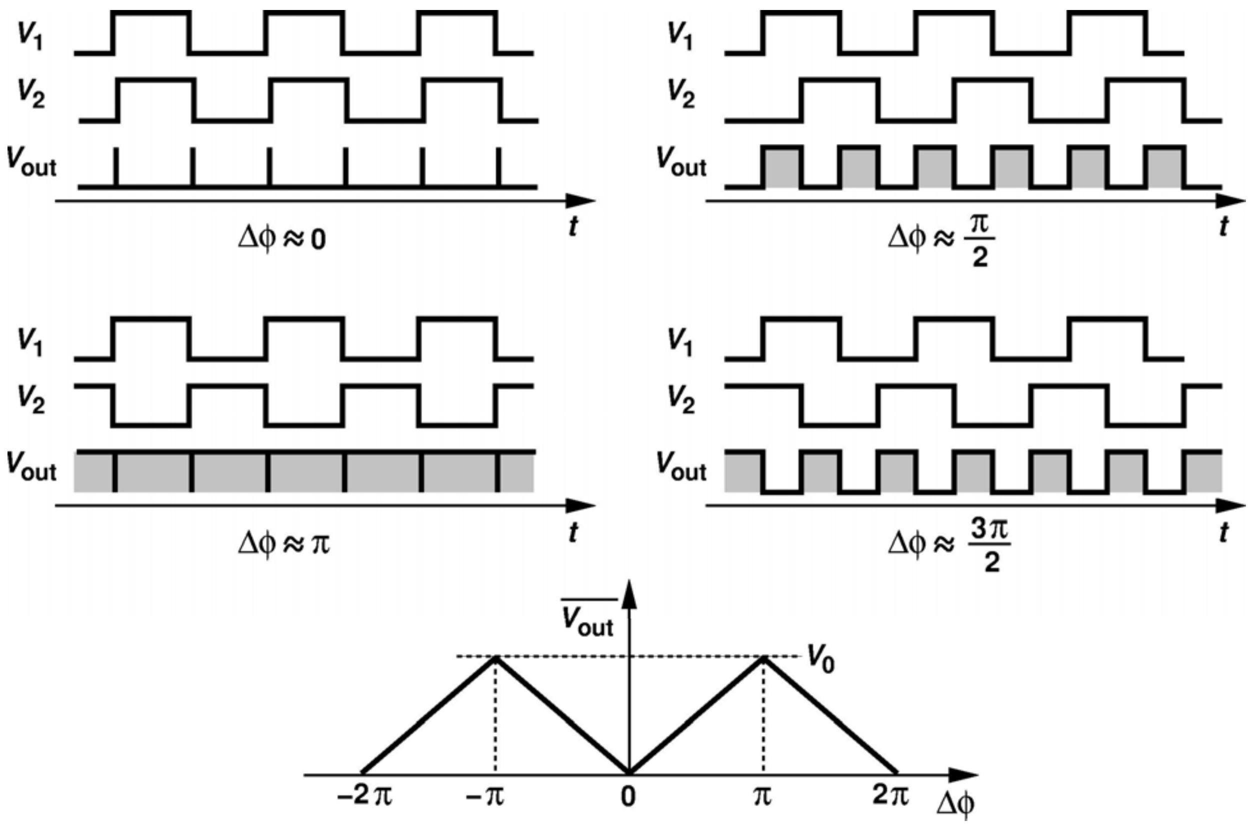
XOR Gate as a Phase Detector





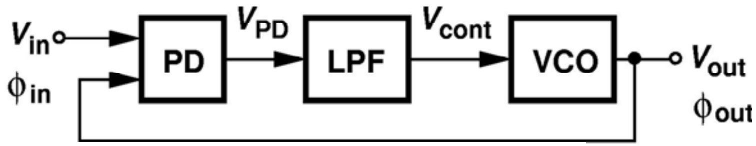
- An XOR gate can serve as a phase detector by examining the difference of rising/falling times.
- Work only for periodic signals.

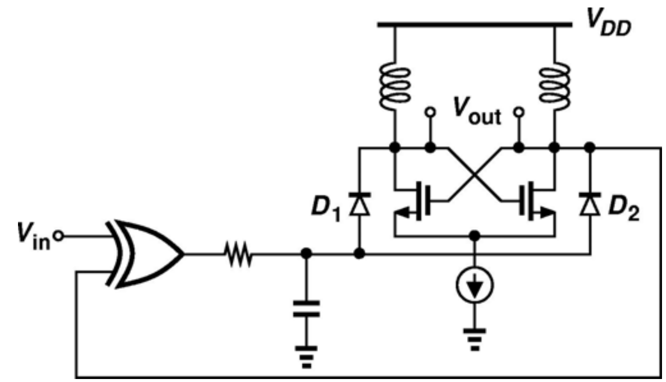
Response of XOR as a Phase Detector



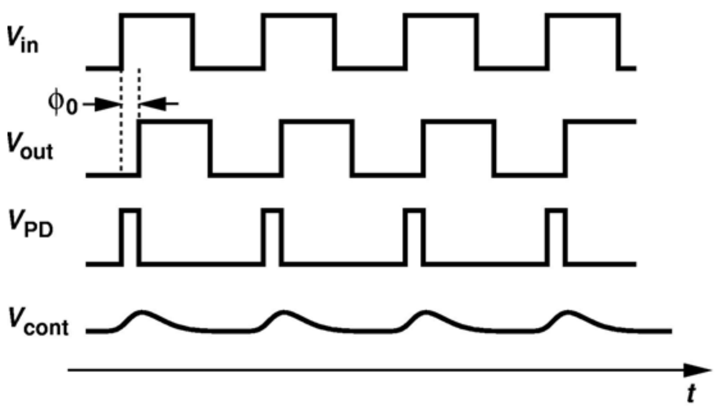
- **Periodic input/output characteristic implies limited capture range. (Why?)**

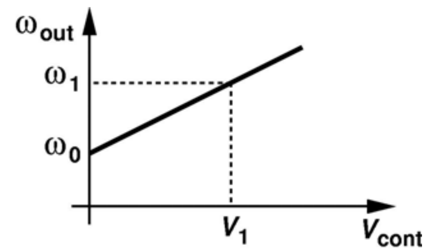
Simple PLL

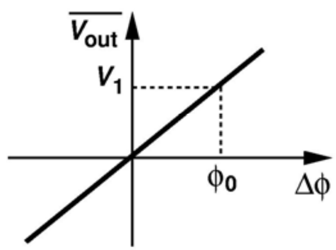




$$\omega_{out} = \omega_{in}$$

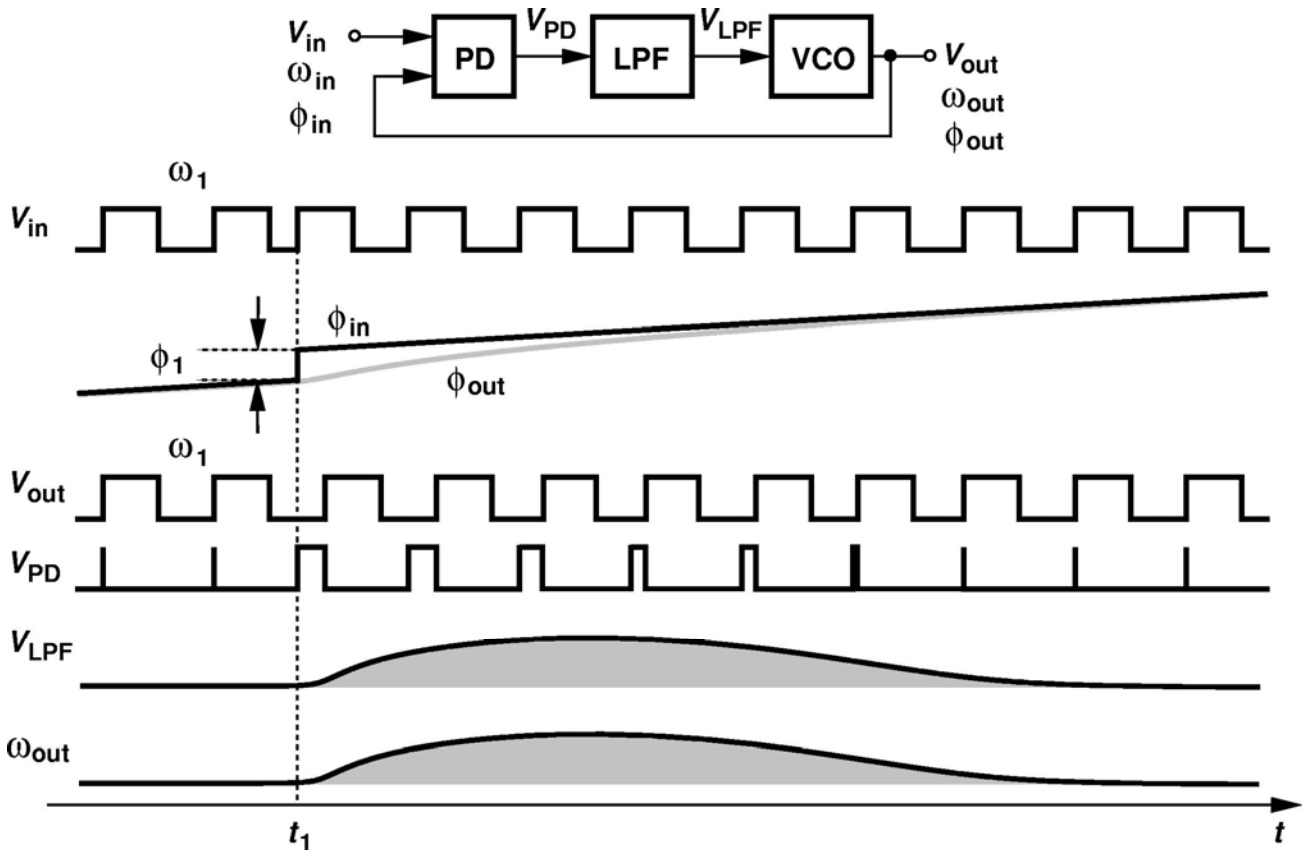






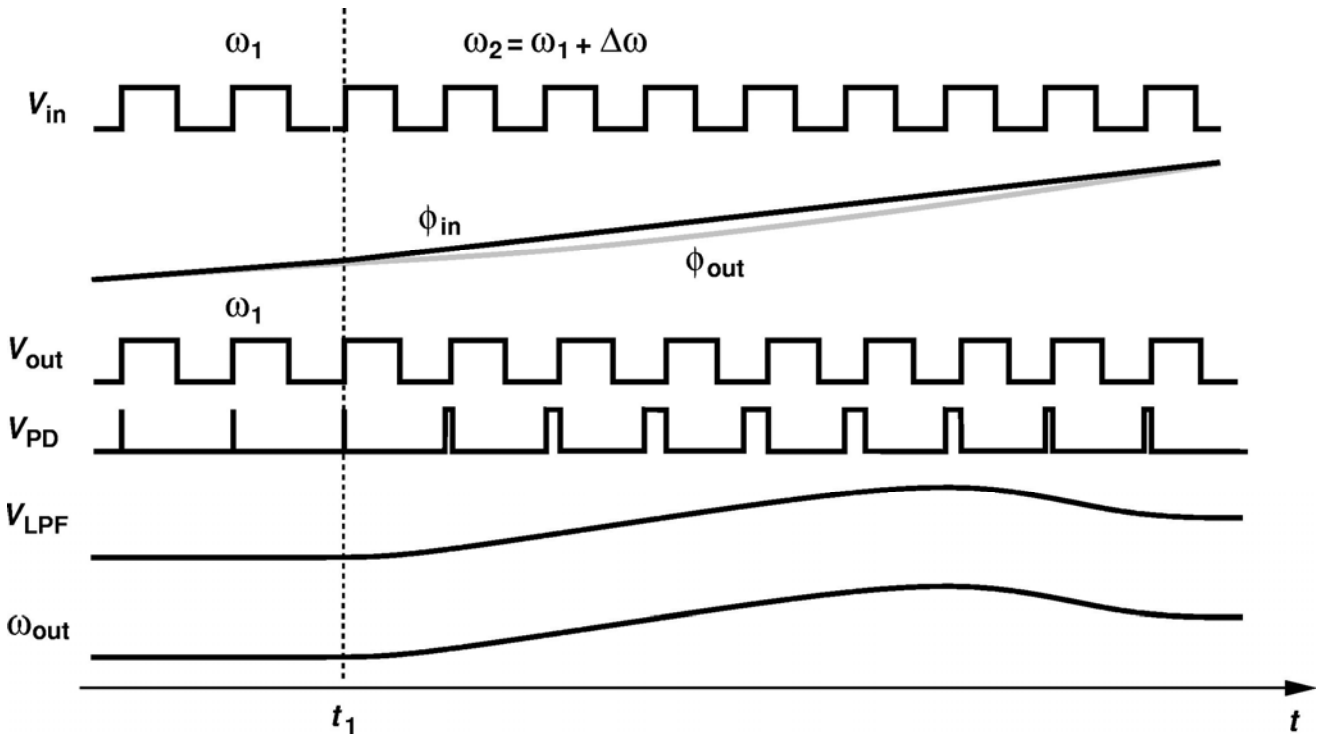
- Phase relationship is undetermined.

Response of Simple PLL to a Phase Step



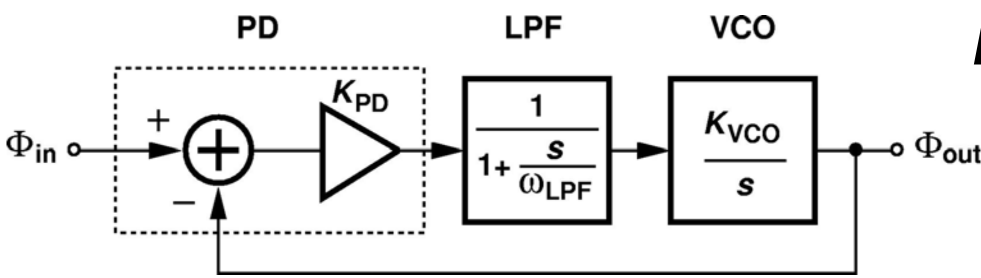
- Integration of the shadow part of ω_{out} equals ϕ_1.

Response of Simple PLL to a Frequency Step



- ω_{out} changes from ω_1 to ω_2 eventually.
- V_{PD} changes as well.

Dynamic Behavior of Simple PLLs



$$H(s)\Big|_{open} = \frac{\Phi_{out}}{\Phi_{in}}(s)\Big|_{open}$$

$$= K_{PD}\frac{1}{1+\frac{s}{\omega_{LPF}}}\frac{K_{VCO}}{s}$$

$$H(s)\Big|_{closed} = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}}$$

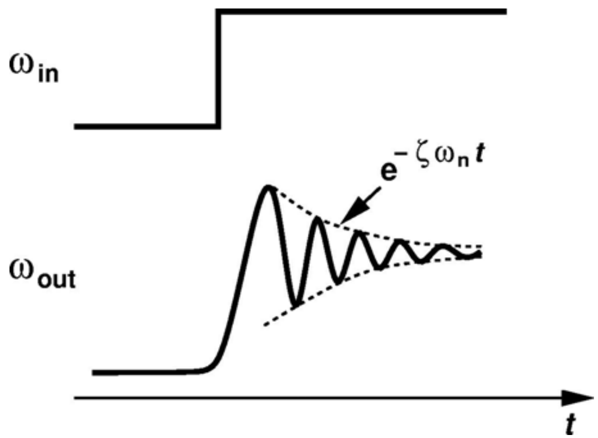
$$= \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\omega_{LPF}K_{PD}K_{VCO}}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}$$

- Typical second order transfer function.

Dynamic Behavior of Simple PLLs

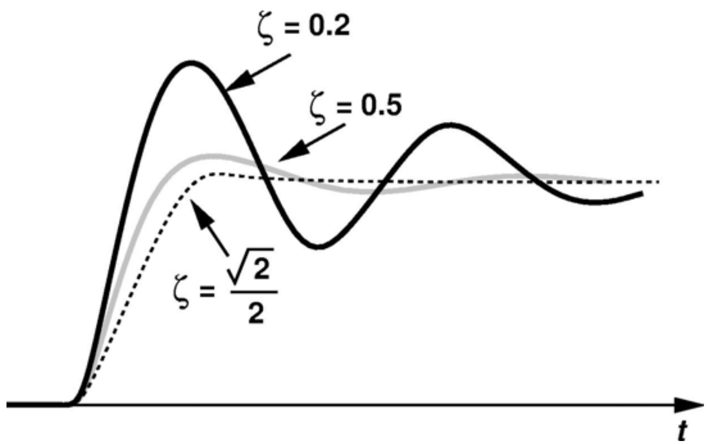


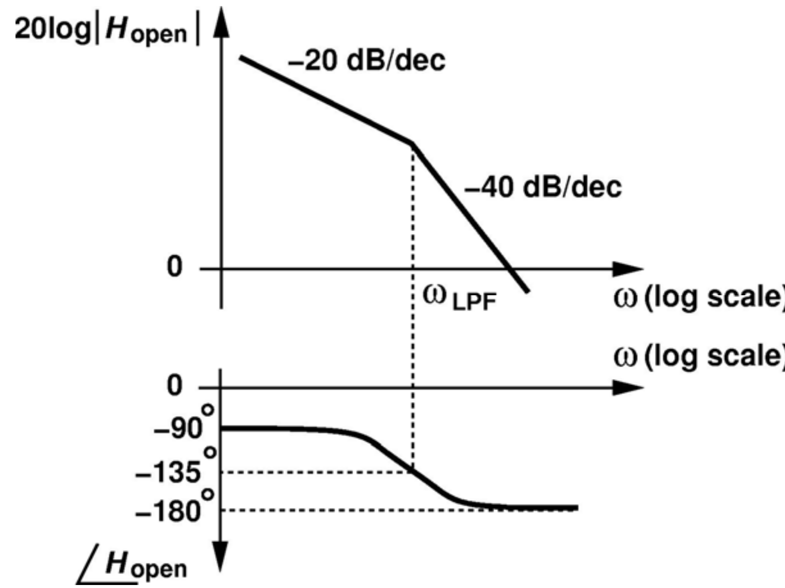
$$s_{1,2} = (-\zeta \pm \sqrt{\zeta^2 - 1})\omega_n$$

$$\zeta\omega_n = \frac{1}{2}\omega_{LPF}$$

- Decaying envelope determines the settling time.
- Settling time and noise suppression present a critical trade-off.
- RF applications usually require an under- or critical-damped response.

Stability of Simple PLLs



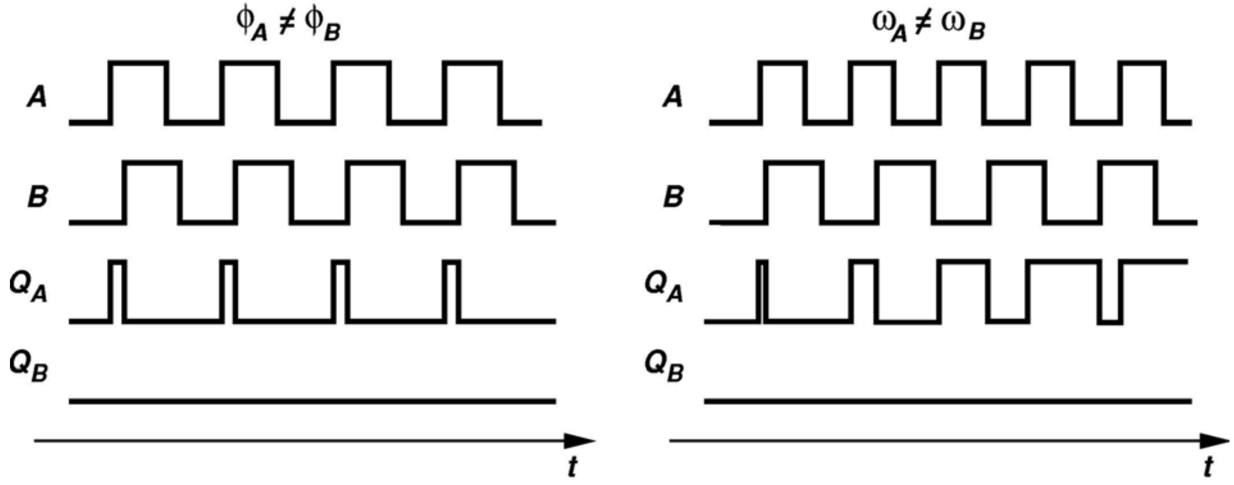


- Small ζ leads to ringing (unstability).
- For 45° phase margin, $K_{PD}K_{VCO} = \sqrt{2}\,\omega_{LPF}$

Charge-Pump PLLs

- Simple PLL suffers from numbers of drawbacks that prohibit it from high-performance applications:
  - critical trade-off between settling and noise
  - finite and undetermined phase error
  - limited acquisition range
- Charge-pump PLLs can relax the tradeoffs, and produce zero phase error.
- Large acquisition range can be achieved by introducing frequency acquisition loop.

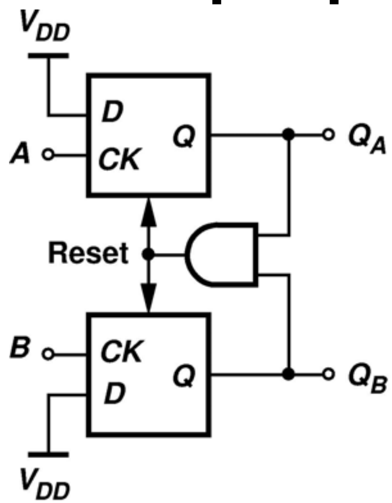
Phase/Frequency Detector (PFD)

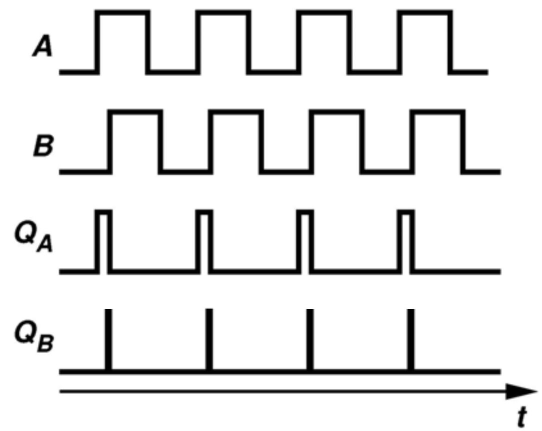


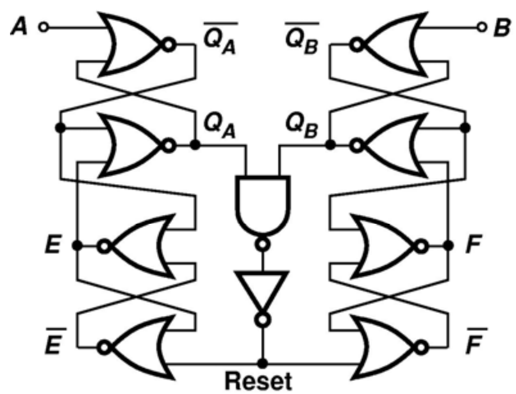
- For periodic signals, phase and frequency acquisition can be merged.
- Necessitating reset technique.

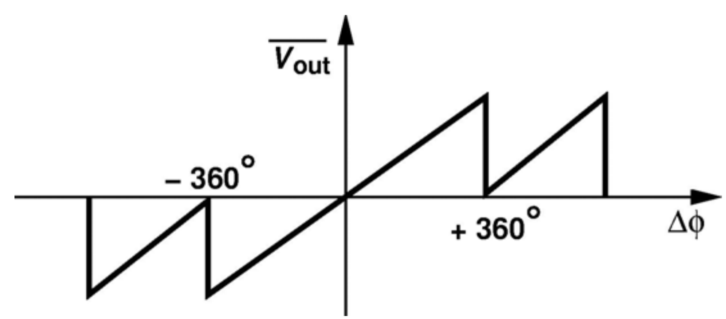
Linear PFD

- Linear PFD detects the phase (frequency) error and generates an output proportional to the difference.



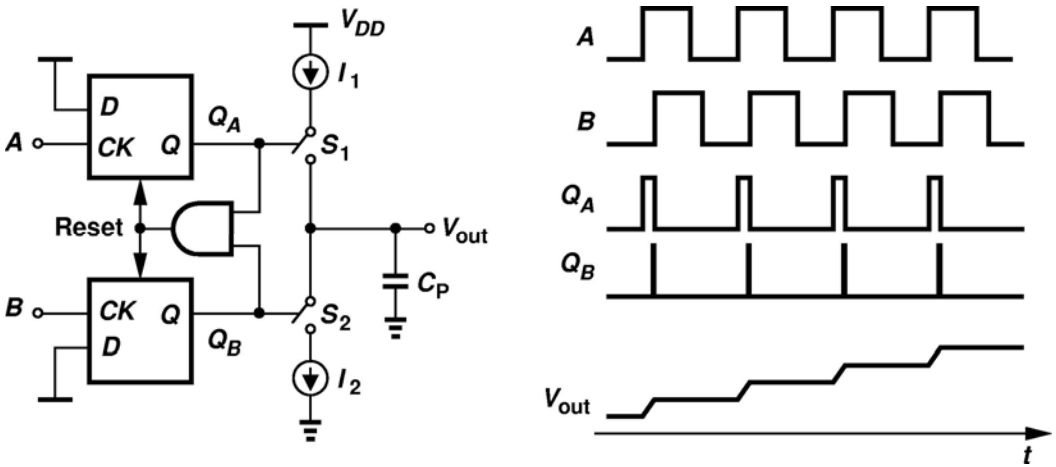


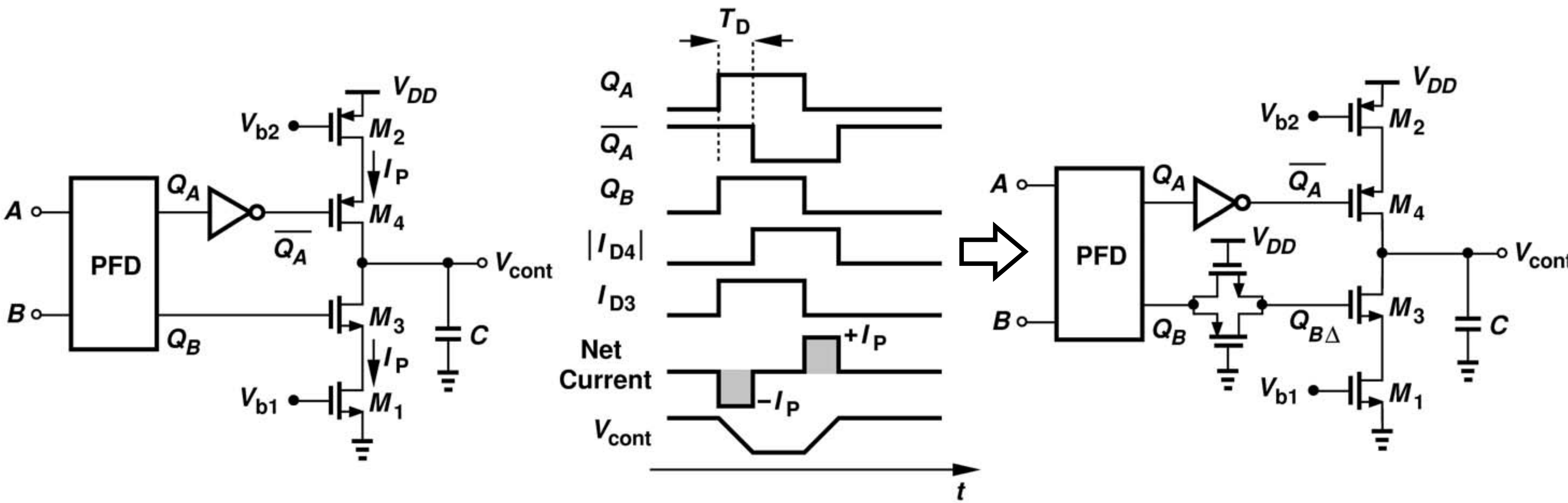




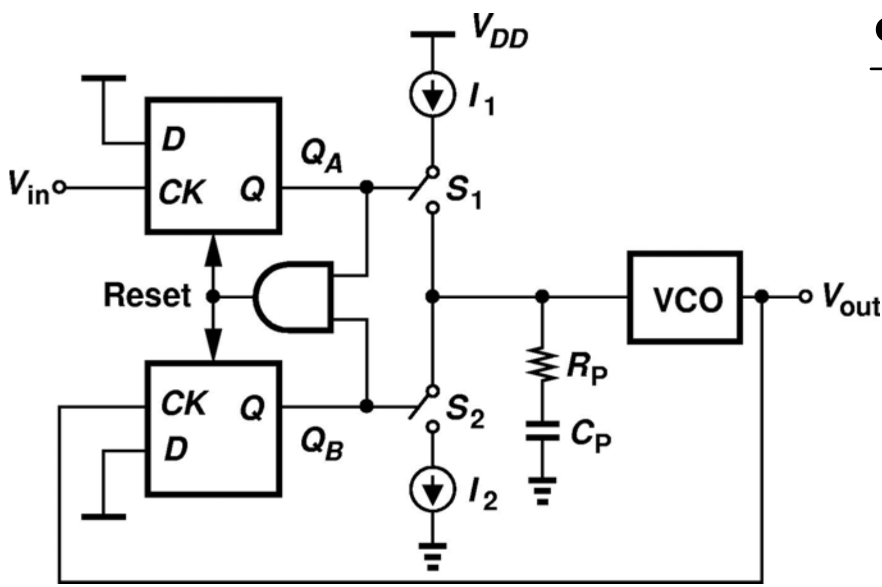
- Non-periodic characteristic suggests infinite capture range because it "swallows" extra pulse if needed.

Linear PFD with Charge Pump





Dynamic Behavior of Charge-Pump PLLs



$$\frac{\Phi_{out}}{\Phi_{in}}(s)\Big|_{open} = \frac{I_P}{2\pi}\left(R_p + \frac{1}{C_P s}\right)\frac{K_{VCO}}{s}$$

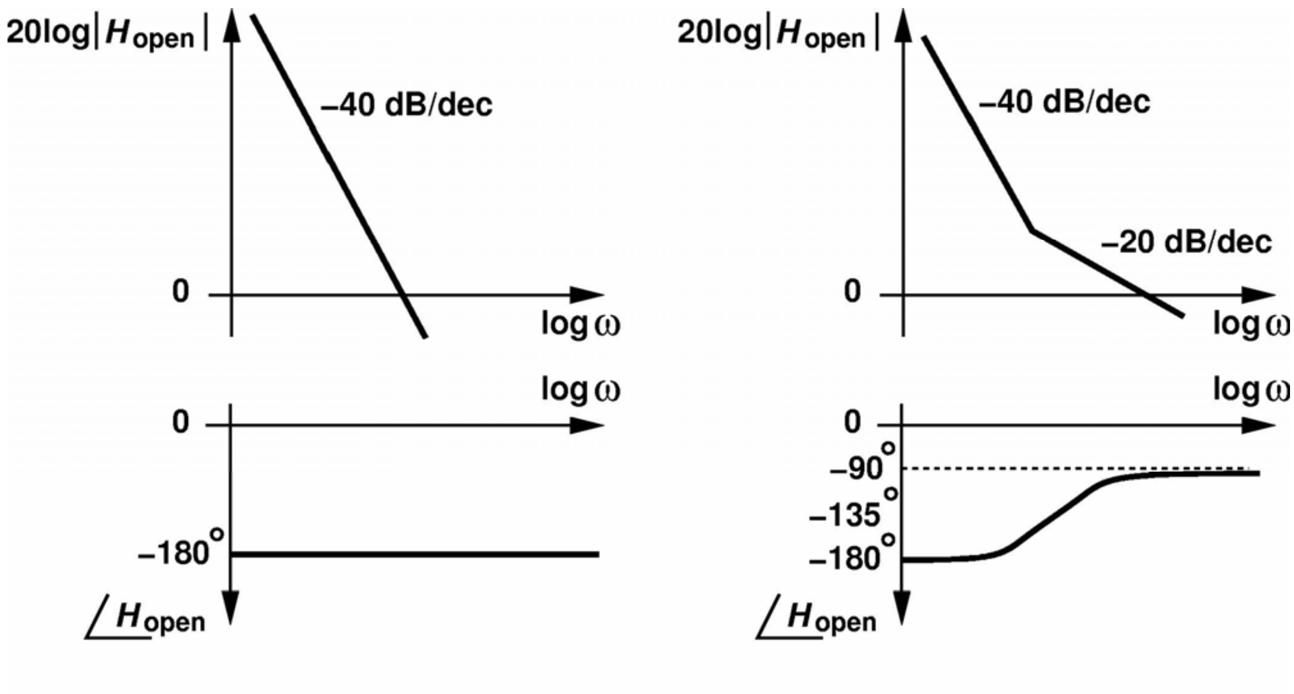
$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_P}}$$

$$\zeta = \frac{R_P}{2}\sqrt{\frac{I_P C_P K_{VCO}}{2\pi}}$$

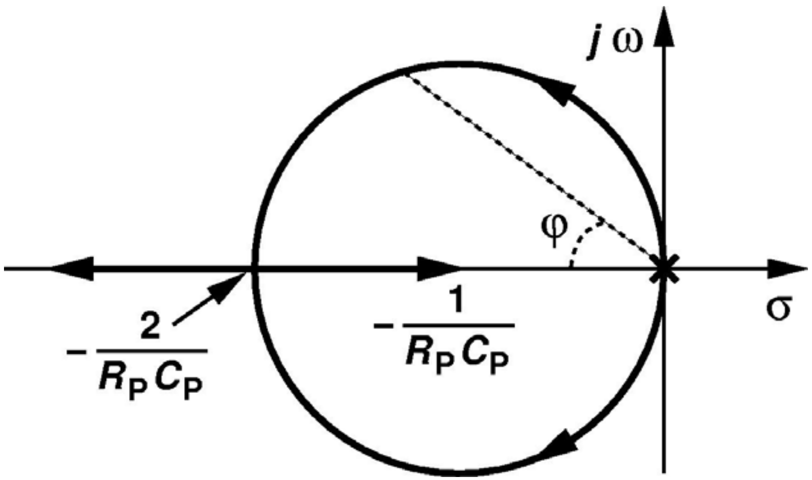
❐ **Resistor R_P must be introduced to create a zero.**

Comparison of 1st and 2nd Order PLLs



- First-order PLLs are unconditionally unstable.
- Second-order can be stable if proper design applies.

Root Locus of 2nd Order PLLs

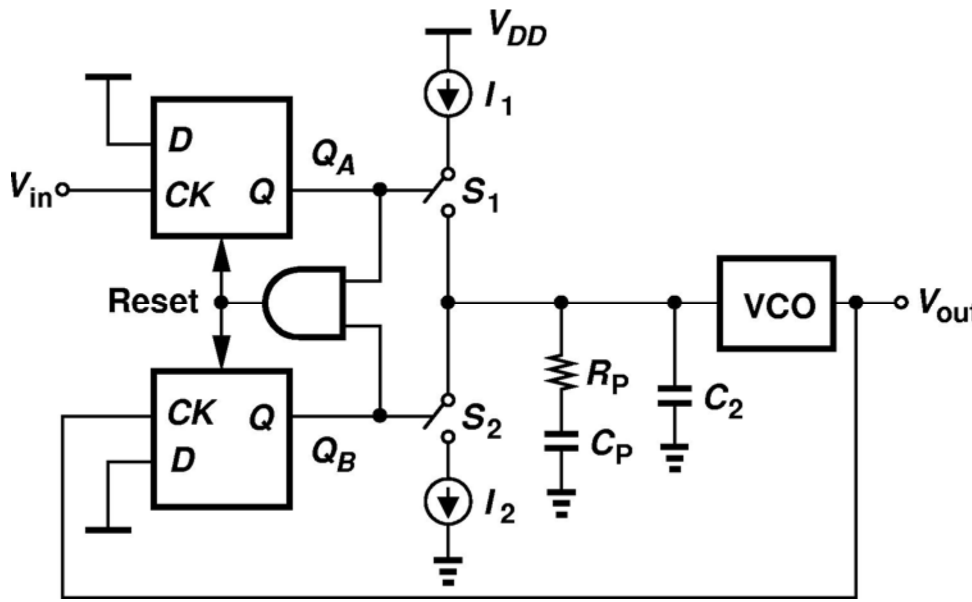


$$s_{1,2} = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$$

$$\zeta = \cos\psi$$

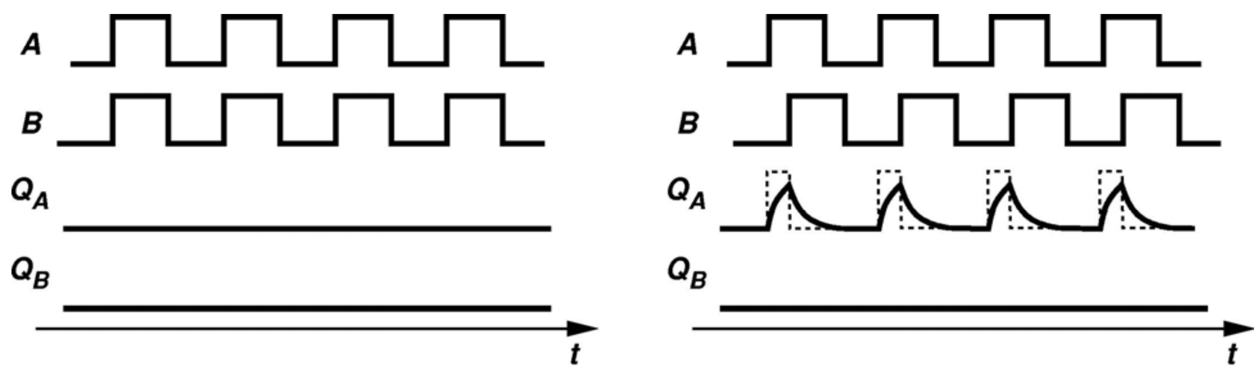
- The two poles split at origin, go around a circle, merge again at $-\frac{2}{R_P C_P}$, and finally move along the real axis in opposite directions.

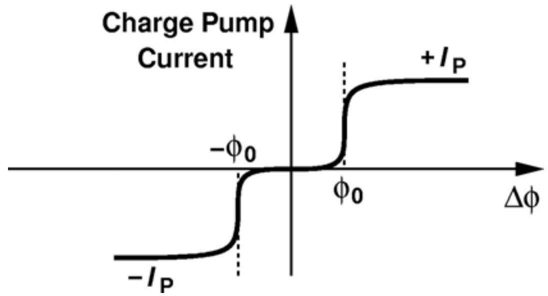
Third-Order Charge Pump PLLs

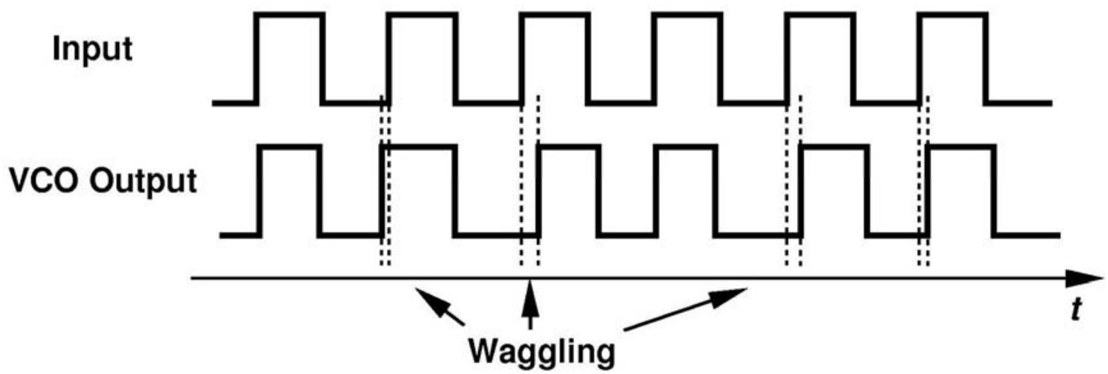


- VCO control line experiences a large jump due to current charging or discharging through R_P.
- A small capacitor C_2 is therefore introduced to suppress the ripple.
- It should impose only negligible influence on loop parameters.

Dead-Zone in PFD & Charge Pump

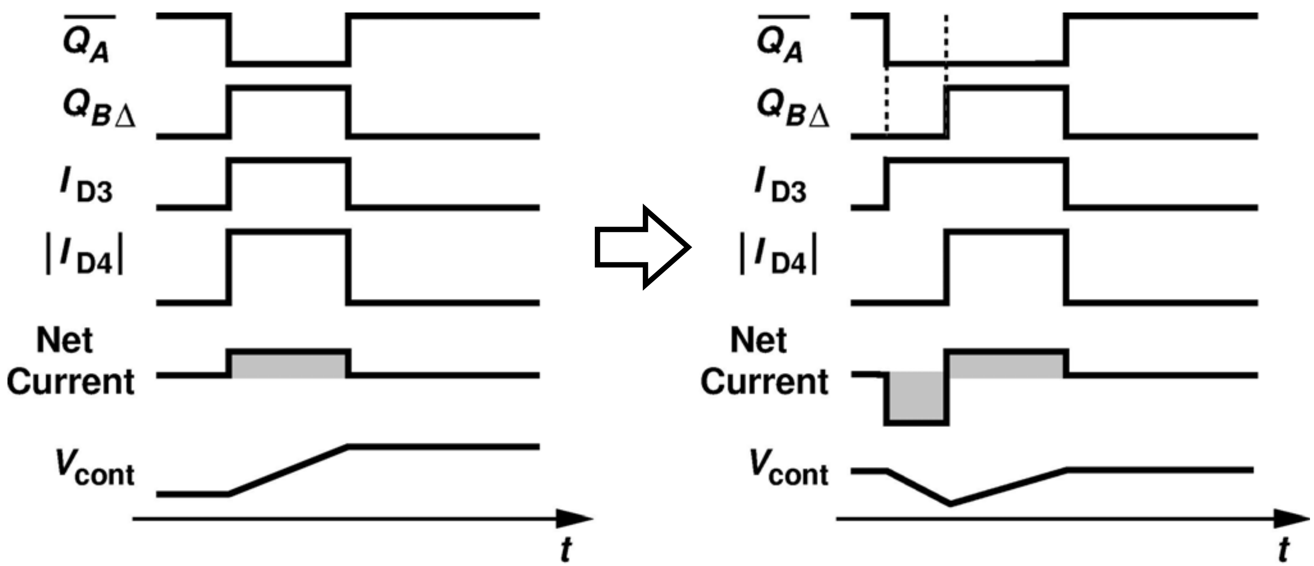






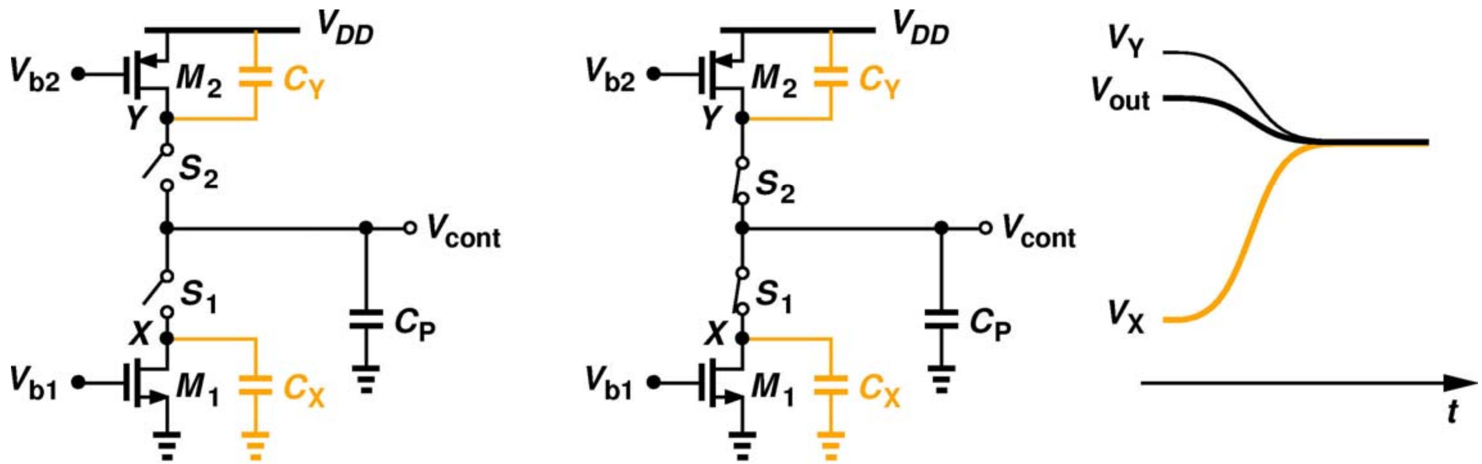
- ❐ A PFD/CP circuit provides no corrective feedback, leading to substantial jitter.
- ❐ Fortunately, type IV PFD produces coincident pulses and dead-zone issue is eliminated.

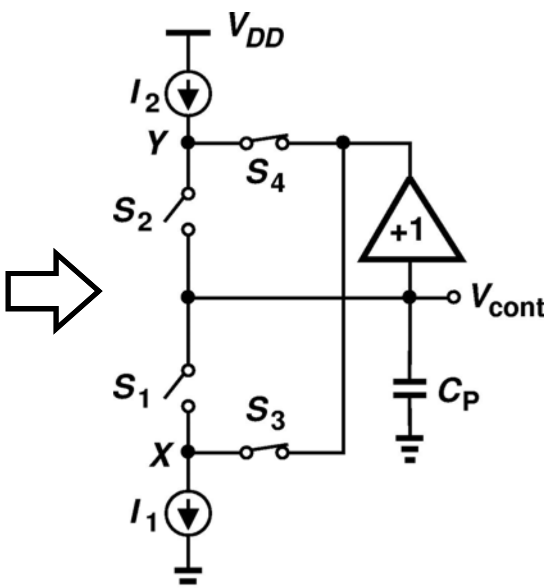
Current Mismatch Issue in Charge Pumps



- Periodic ripple on VCO control line are observed due to current mismatches and/or channel-length modulation.
- Control line ripple induces spurs (sidebands) directly.

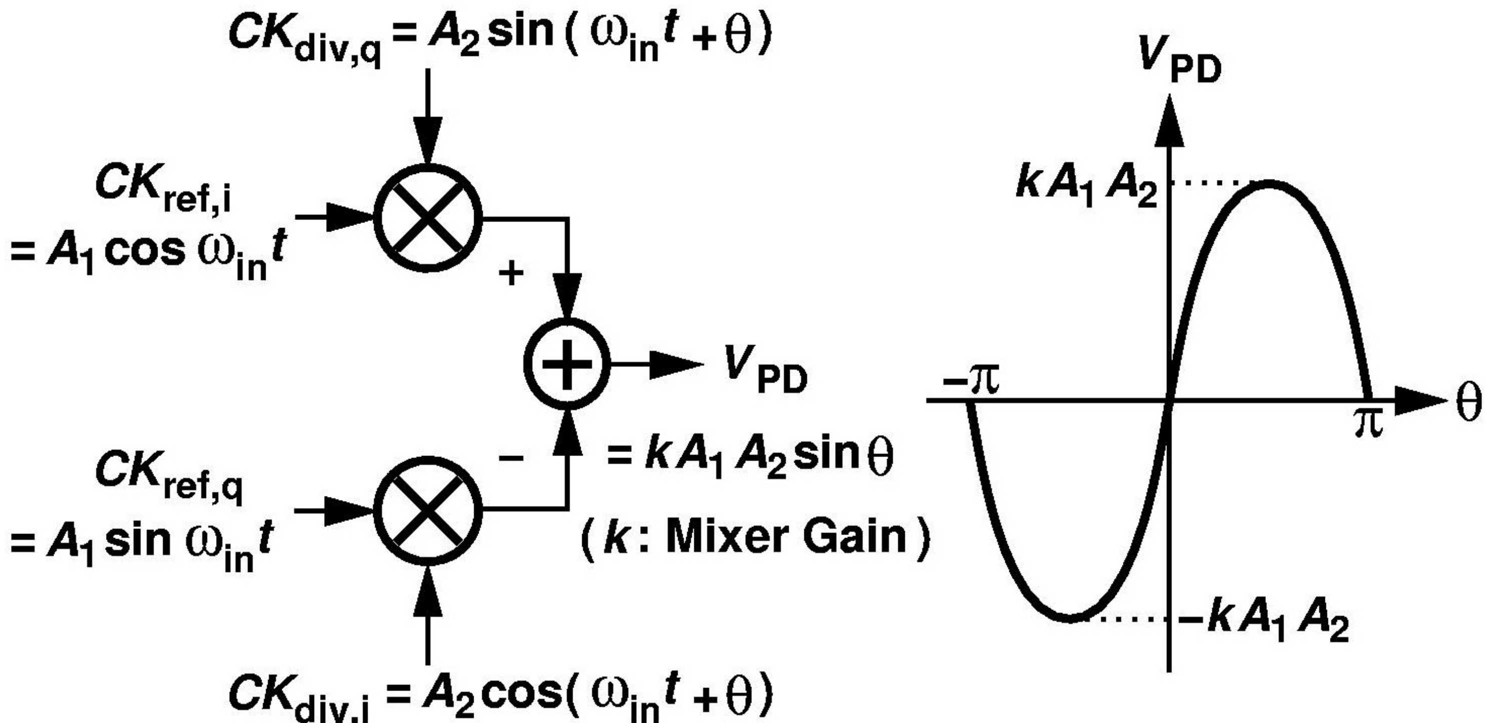
Charge Sharing Issue in Charge Pumps





- ❐ Charge equalization can be used during idle time to minimize the effect.
- ❐ Charge injection of the switches still cause mismatches.

Case Study - SSB-Based Phase Detector



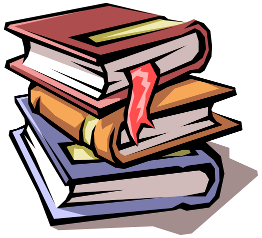
[Lee, ISSCC07]

- Near-dc output V_{PD} applies to $(V/I)_{PD}$.
- Finite image would appear at $2\omega_{in}$.

Frequency Synthesizers

Professor Jri Lee

台大電子所　李致毅教授



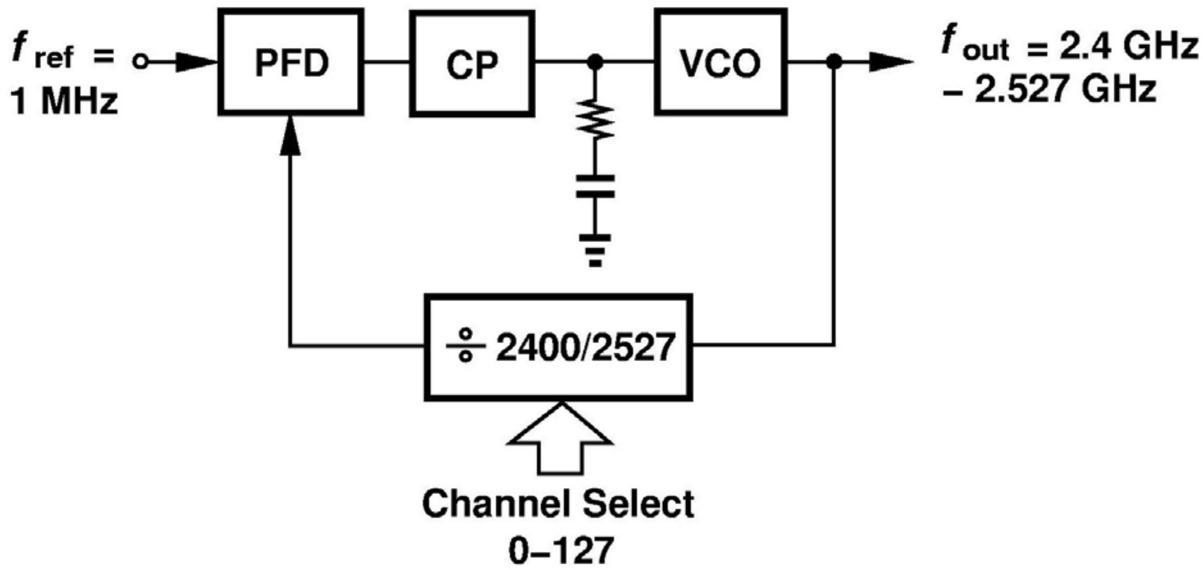
Electrical Engineering Department

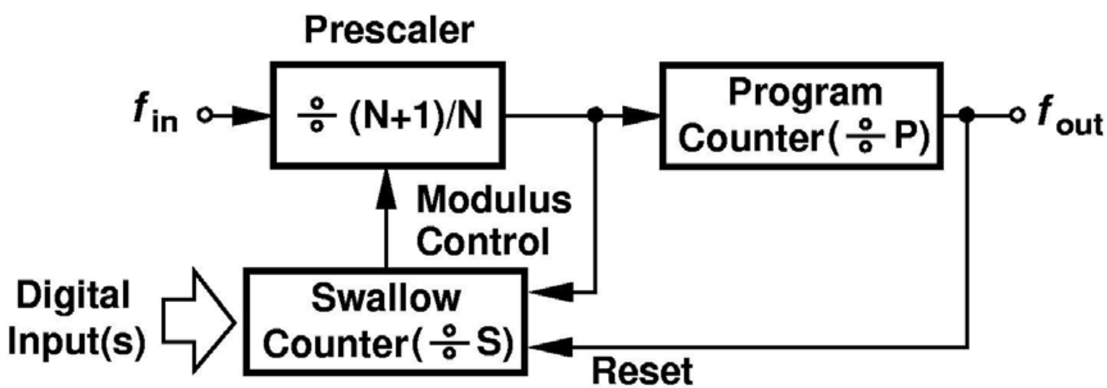
National Taiwan University

Outline

- Introduction
- Integer-N Synthesizer
- Fractional-N Synthesizer
  - Accumulator-Based
  - $\Sigma-\Delta$ Modulated
- Direct Digital Synthesizer
- Case Study

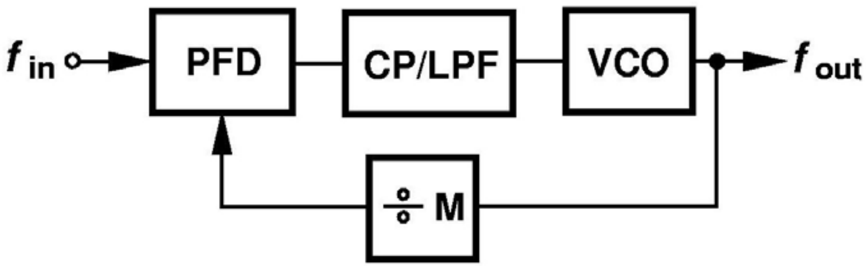
Integer-N Synthesizers





$$f_{out} = \frac{f_{in}}{NP+S}$$

Introducing Divide Ratio M



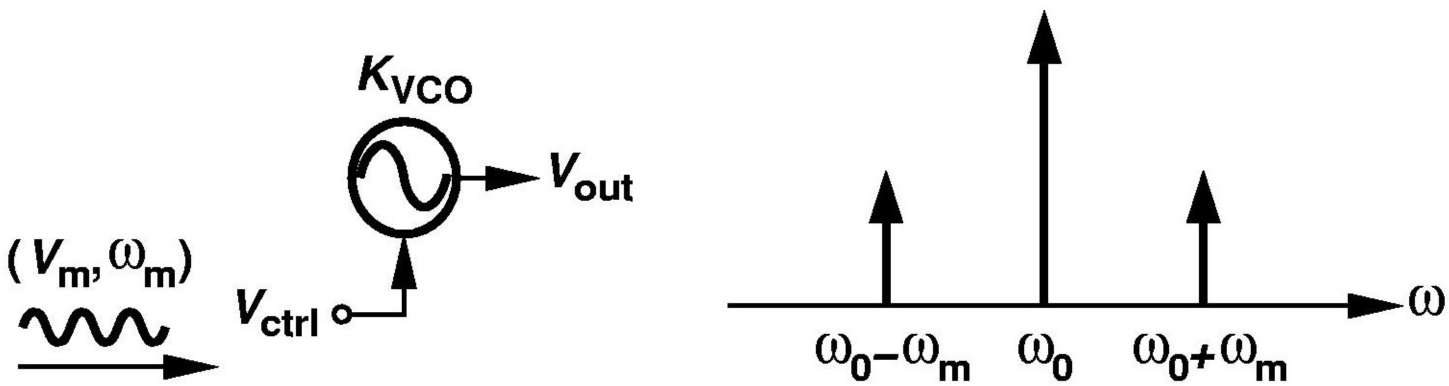
$$H(s)=\frac{\dfrac{I_pK_{VCO}}{2\pi C_p}(R_pC_ps+1)}{s^2+\dfrac{I_p}{2\pi}\dfrac{K_{VCO}}{M}R_ps+\dfrac{I_p}{2\pi C_p}\dfrac{K_{VCO}}{M}}$$

$$\omega_n=\sqrt{\frac{I_p}{2\pi C_p}\frac{K_{VCO}}{M}}\quad,\ \xi=\frac{R_p}{2}\sqrt{\frac{I_pC_p}{2\pi}\frac{K_{VCO}}{M}}$$

Decay $\tau=(\xi\omega_n)^{-1}=\dfrac{4\pi M}{R_pI_pK_{VCO}}$

- **Settling time** $\propto\dfrac{1}{\xi\omega_n}\Leftarrow$ **critical in channel selection.**
- **Closed-loop synthesizer fails to serve in special applications such as frequency hopping and instant locking.**

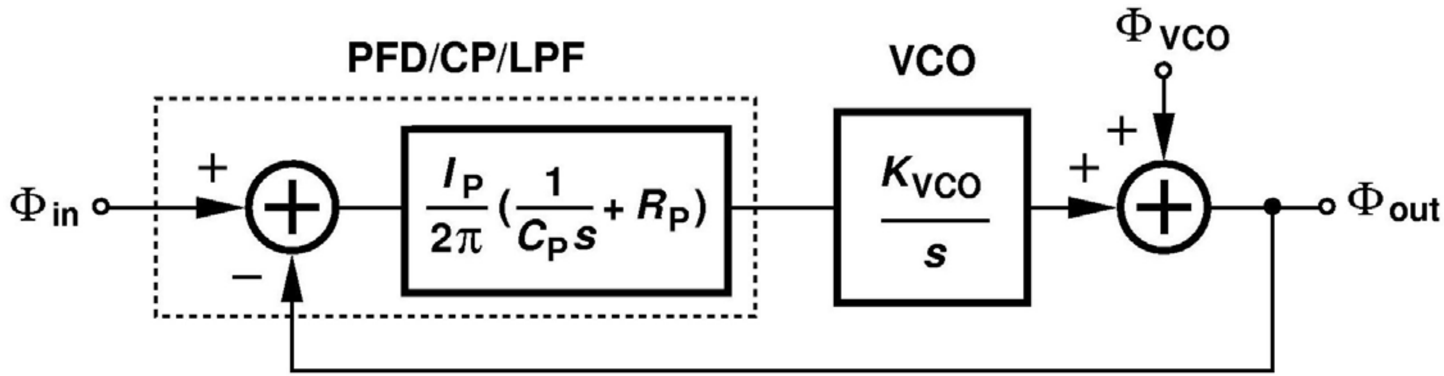
Reference Feedthrough and Sidebands

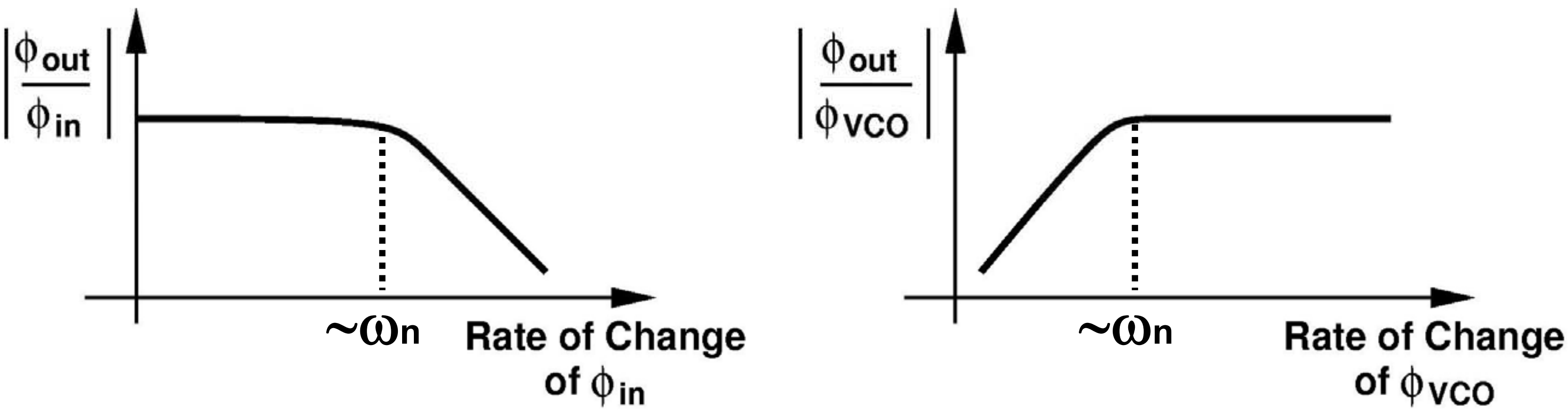


$$V_{out}(t) \cong A_0 \cos\omega_0 t + \frac{A_0 V_m K_{VCO}}{2\omega_m}[\cos(\omega_0 + \omega_m)t - \cos(\omega_0 - \omega_m)t]$$

- **Control line ripple introduces jitter too (how to estimate it?)**
- **Sidebands interfere with adjacent channels.**

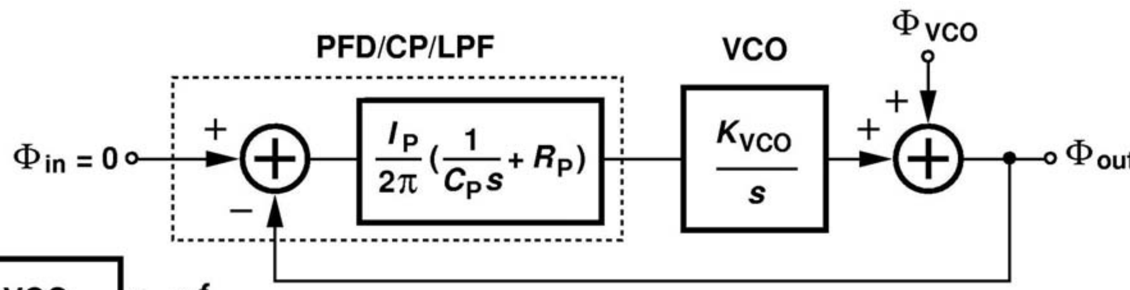
Noise Transfer Function

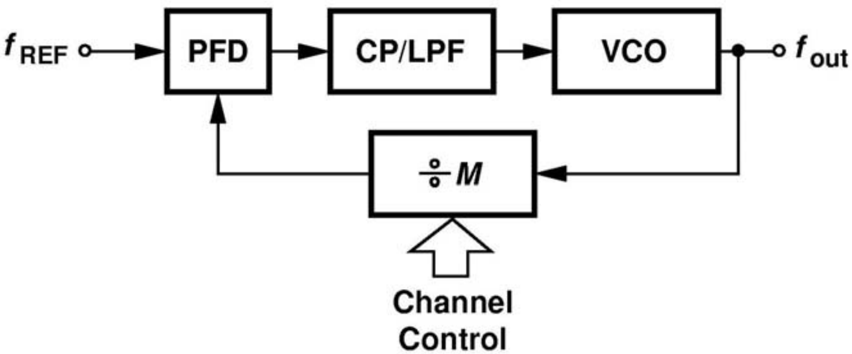




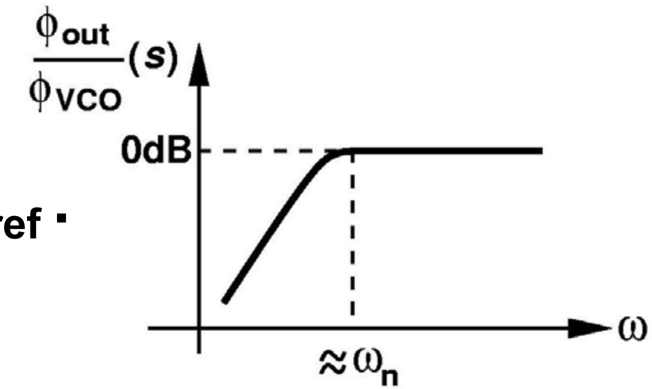
- **Input and VCO noise shaped by low-pass and high-pass filtering with loop bandwidth (~ω_n).**

Limitation of Integer-N Synthesizers





$$\frac{\Phi_{out}}{\Phi_{VCO}}(s) = \frac{s^2}{s^2 + 2\xi\omega_n + \omega_n^2}$$



- Loop bandwidth < f_{ref} /10. (why?)
- Channel resolution determined by f_{ref} .

⇒ Very low loop bandwidth.

⇒ Having difficulty in suppressing VCO noise.

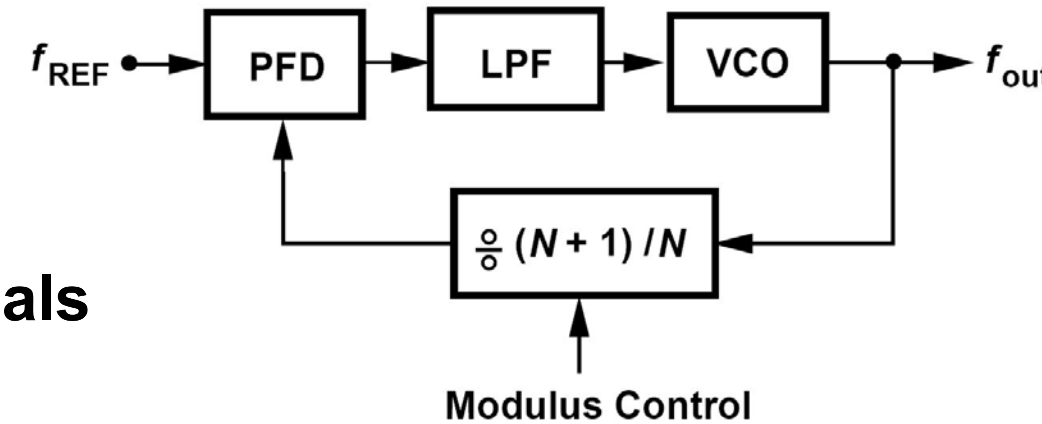
Limitation of Integer-N Synthesizers

- Other issues of integer-N synthesizers:
  - Reference feed-through
  - Finite frequency resolution
  - Large divide ratio
  - High noise floor
- Nonetheless, integer-N is still the most popular one due to its simplicity.
- Do we have any other choice?
  - (Almost) infinite resolution
  - Shaped noise profile
  - Reasonable complexity and power consumption

$\Rightarrow$ **Fractional-N ($\Sigma\Delta$) Synthesizers**

Fractional-N Synthesizers

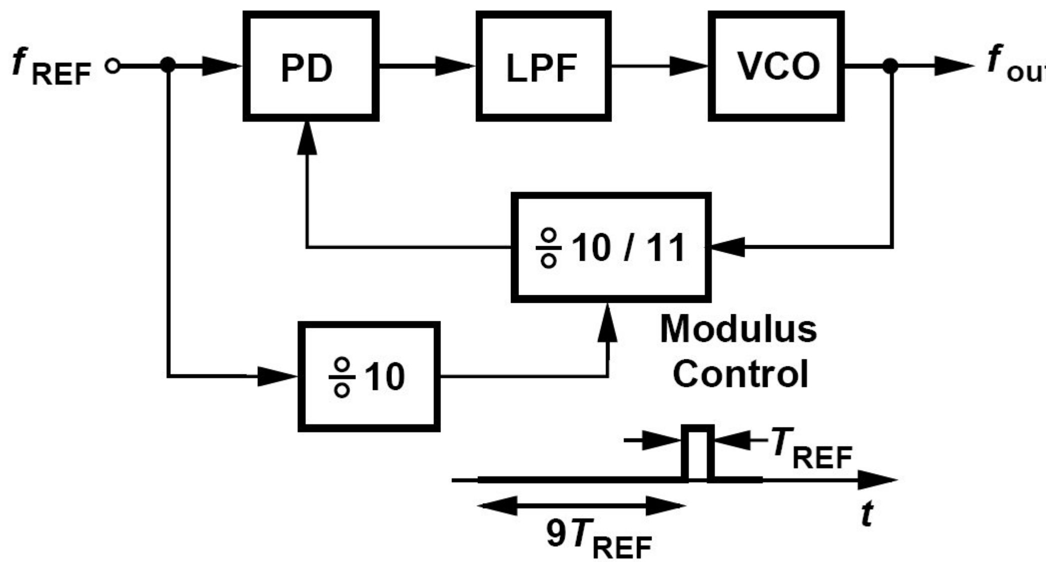
- **Fractional-N**
  - **Modulating the divide ratio such that the averaged modulus equals N+k, where 0 ≤ k ≤ 1**



- **Example:**

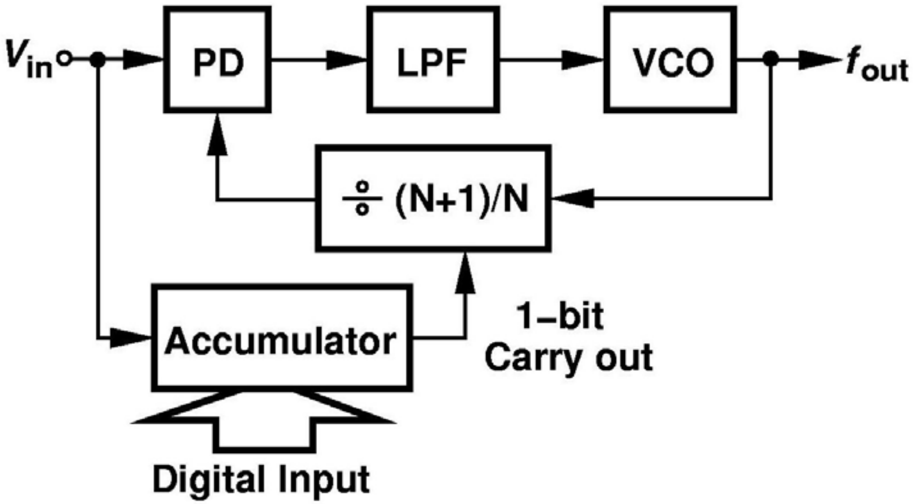
  f_{ref} **= 1 MHz, N = 10**

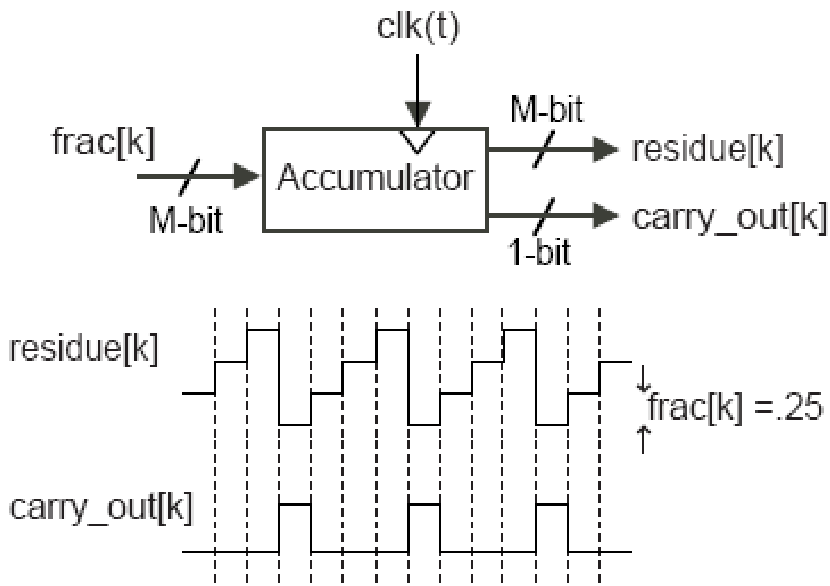
  ⇒ f_{out} **= 10.1 MHz**



Fractional-N Synthesizers

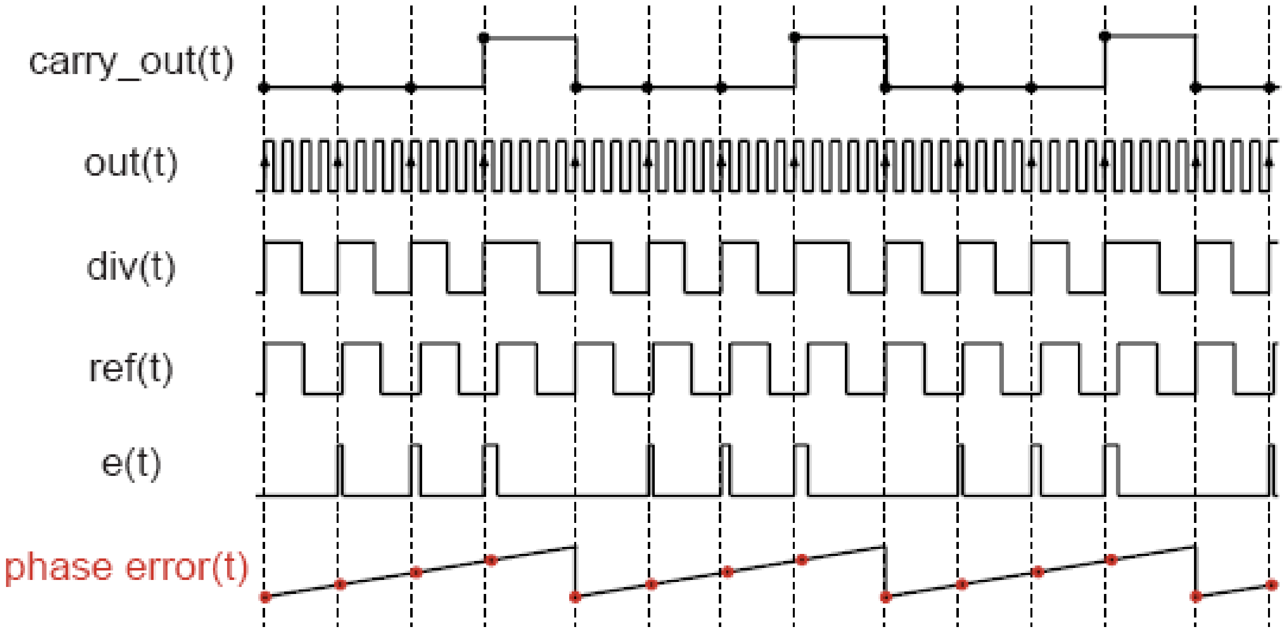
- **Accumulator-Based Fractional-N**





- **Carry out bit asserted whenever overflow happens.**
- **Break constraint of integer divide ratio.**

Example of Accumulator-Based Fractional-N



N=4.25
=(3*4+1*5)/4

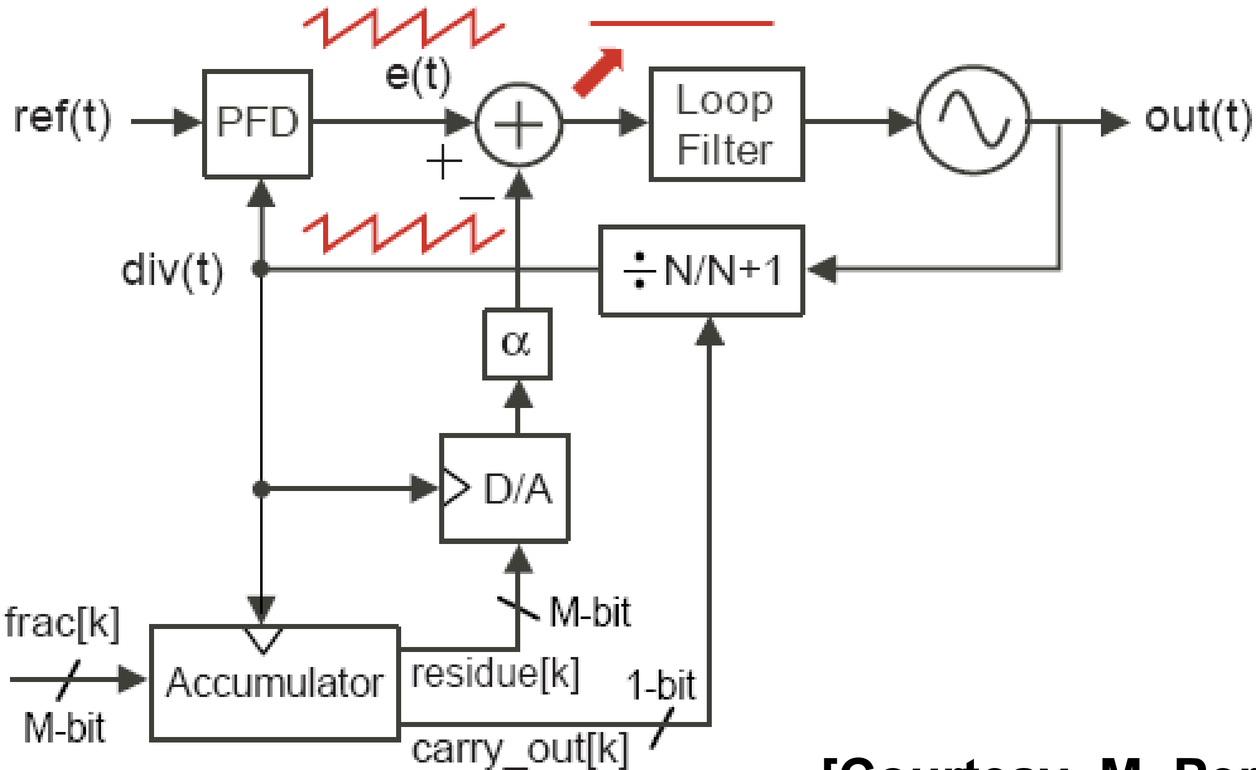
[Courtesy, M. Perrott]

- **Drawback:**
  - **Reference spurs exist since PFD output varies periodically.**

⇒ **Techniques such as phase interpolation could suppress the spurious tones by predicting and canceling the phase error.**

⇒

Ripple Reduction Using Phase Interpolation

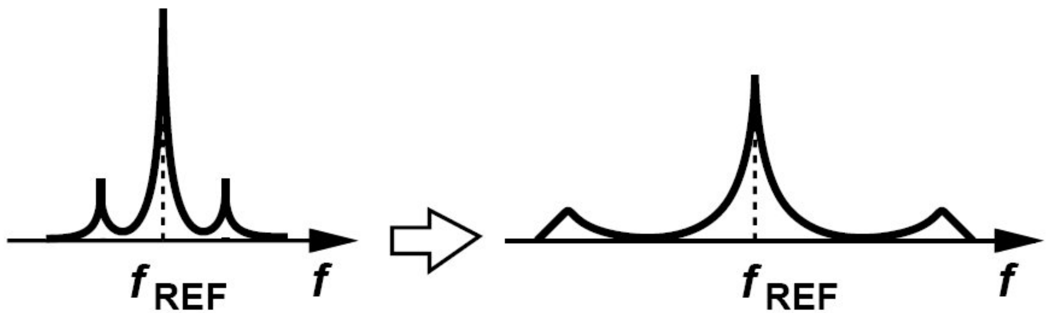


[Courtesy, M. Perrott]

- Phase error cancels based on accumulator residue.

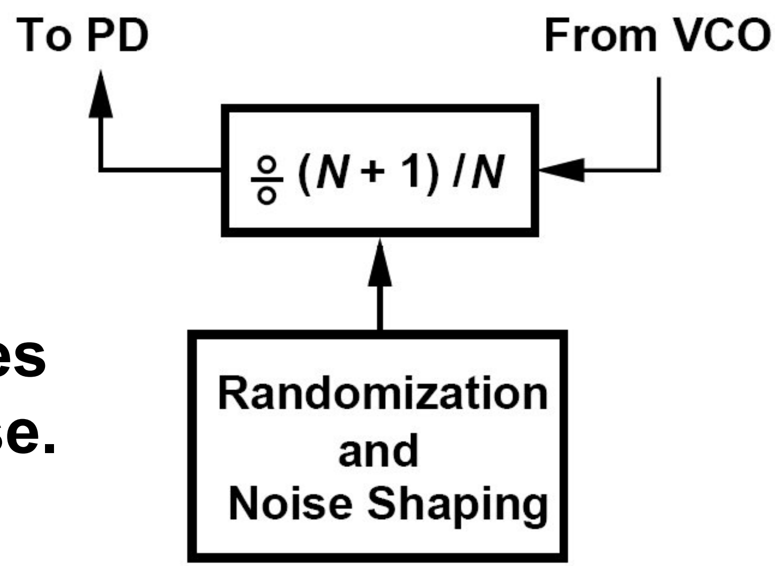
Σ-Δ Modulation

- Noise shaping: pushing quantization noise to high frequencies.



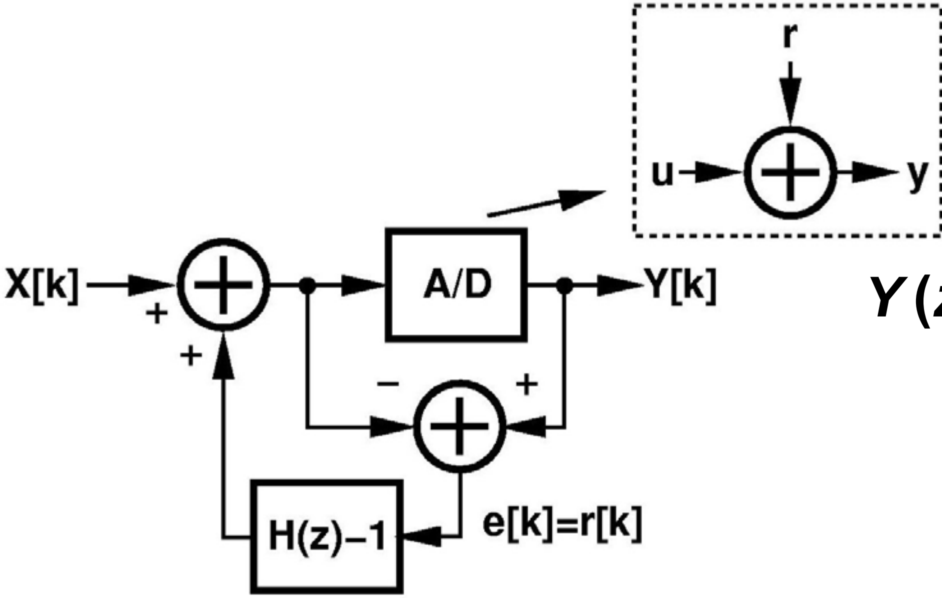
- $S_{nf}(f) \cong \frac{f_{out}^2}{N^4} |Q(f)|^2$

⇒ The PSD of frequency quantization noise resembles that of the quantization noise.



Σ-Δ Modulator

- **Σ–Δ Modulator provides a unity gain path and well-defined noise profile.**



$$
\begin{aligned}
Y(z) &= U(z) + R(z) \\
&= X(z) + [H(z) - 1]E(z) + R(z) \\
&= X(z) + [H(z) - 1]R(z) + R(z) \\
&= X(z) + H(z)R(z)
\end{aligned}
$$

⇒ **Signal Transfer Function (STF) = 1**
Noise Transfer Function (NTF) = H(z)

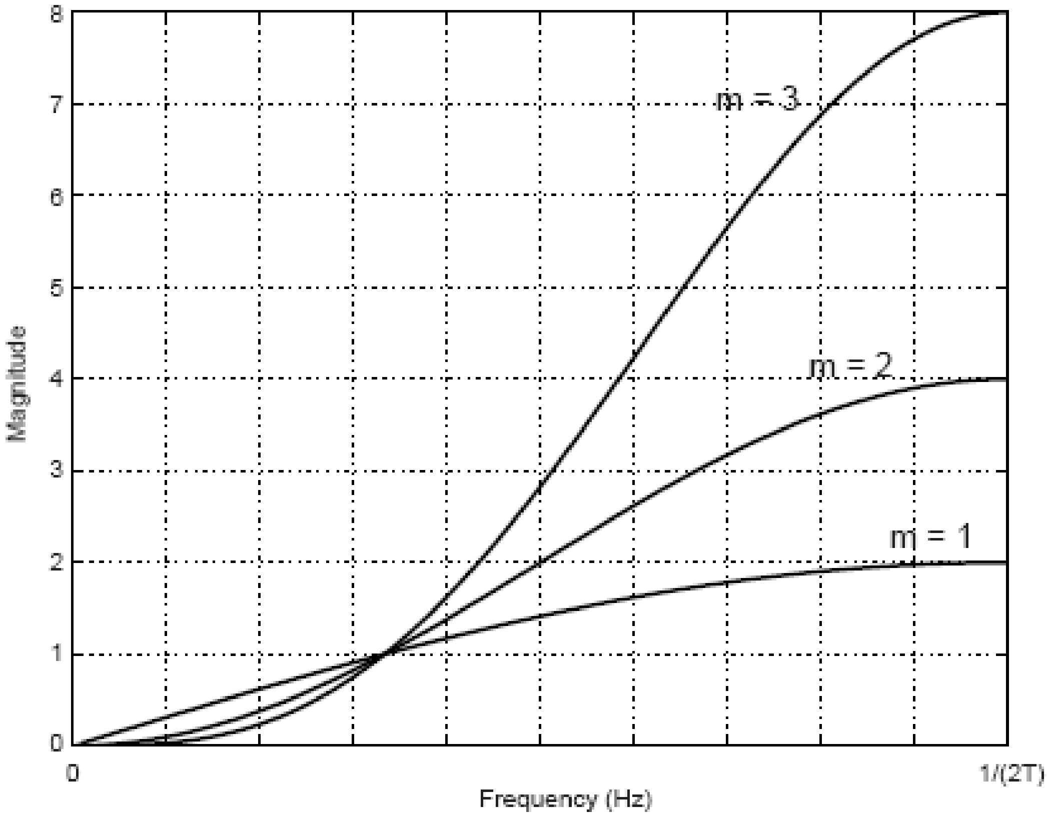
- **Different order gives different shaping.**

Choice of H(z)

$$H(z) = (1 - z^{-1})^m$$

$$\Rightarrow \ |H(e^{j2\pi fT})| = |(1 - e^{-j2\pi fT})^m|$$

← **Easy to implement.**

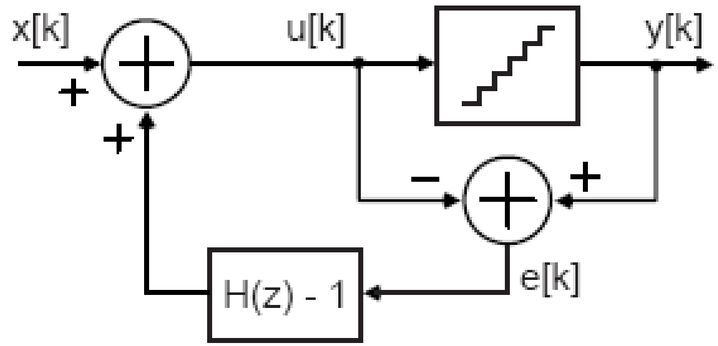


← **Well-defined shaping for different m.**

First-Order Σ-Δ Modulator

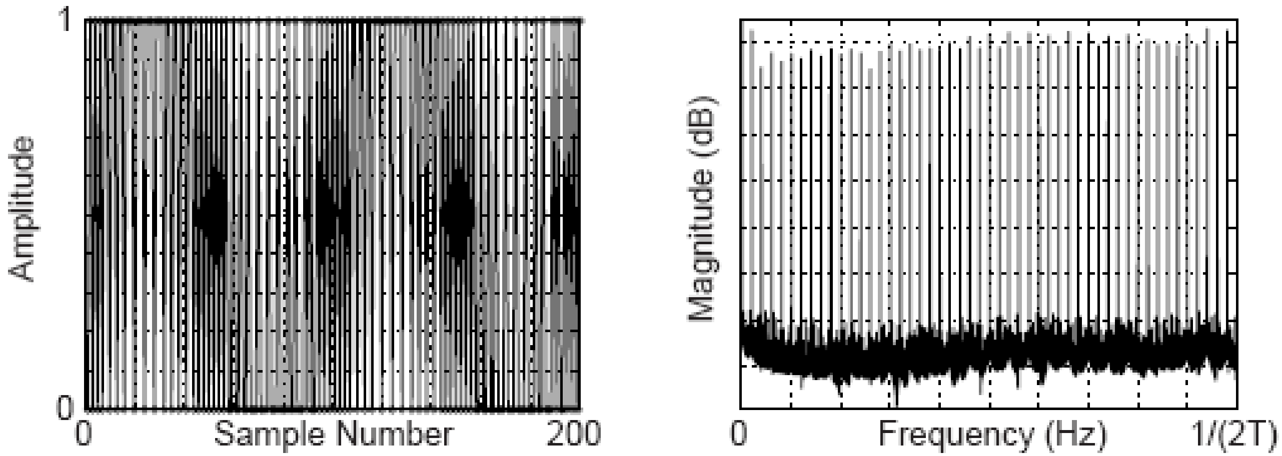
- **Choose NTF to be**

$$H_n(z) = H(z) = 1 - z^{-1}$$



- **Plot of output in time and frequency domains with input of**

$$x[k] = 0.5 + 0.25\sin\left(\frac{2\pi}{100}k\right)$$

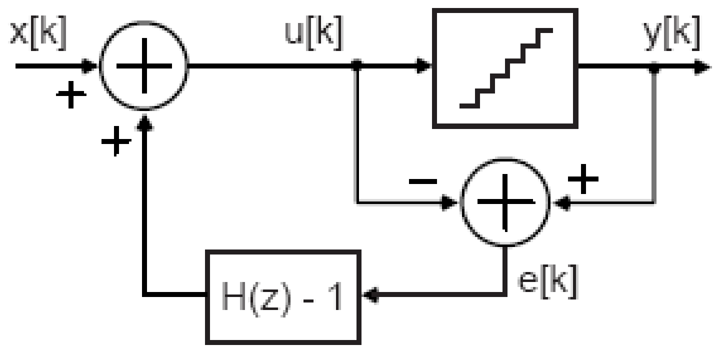


[Courtesy, M. Perrott]

Second-Order Σ-Δ Modulator

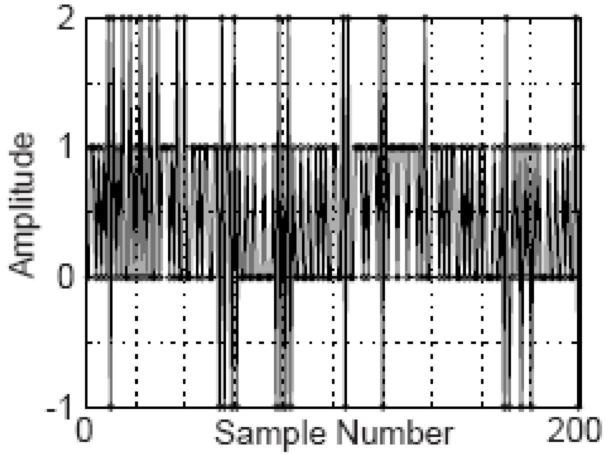
- **Choose NTF to be**

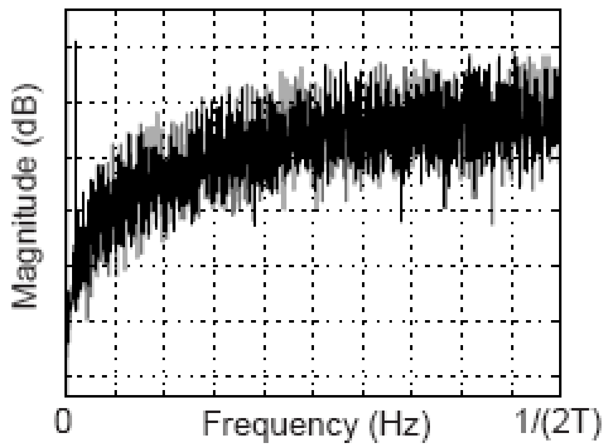
$$H_n(z) = H(z) = (1 - z^{-1})^2$$



- **Plot of output in time and frequency domains with input of**

$$x[k] = 0.5 + 0.25\sin\left(\frac{2\pi}{100}k\right)$$



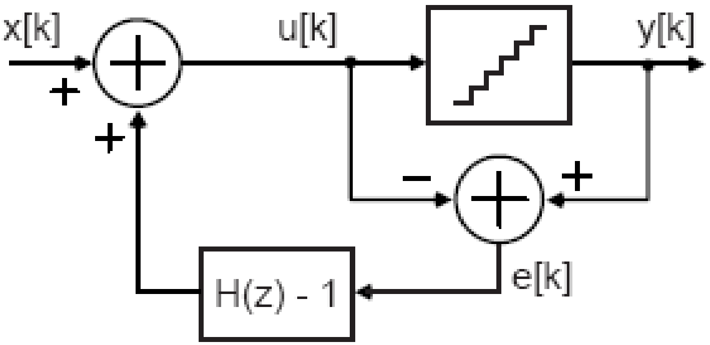


[Courtesy, M. Perrott]

Third-Order Σ-Δ Modulator

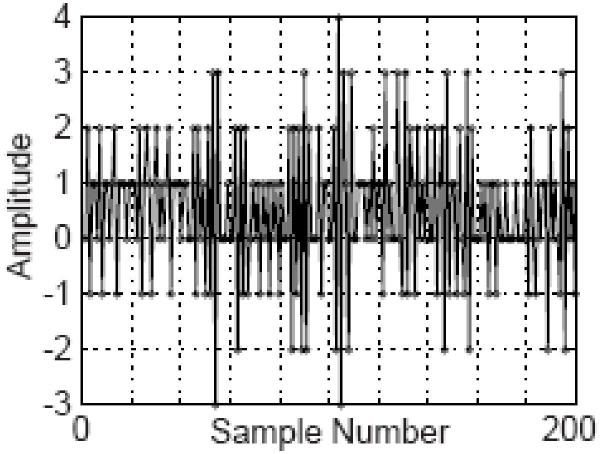
- Choose NTF to be

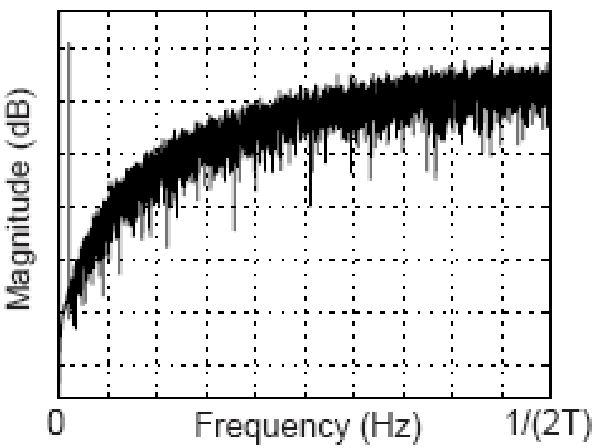
$$H_n(z) = H(z) = (1 - z^{-1})^3$$



- Plot of output in time and frequency domains with input of

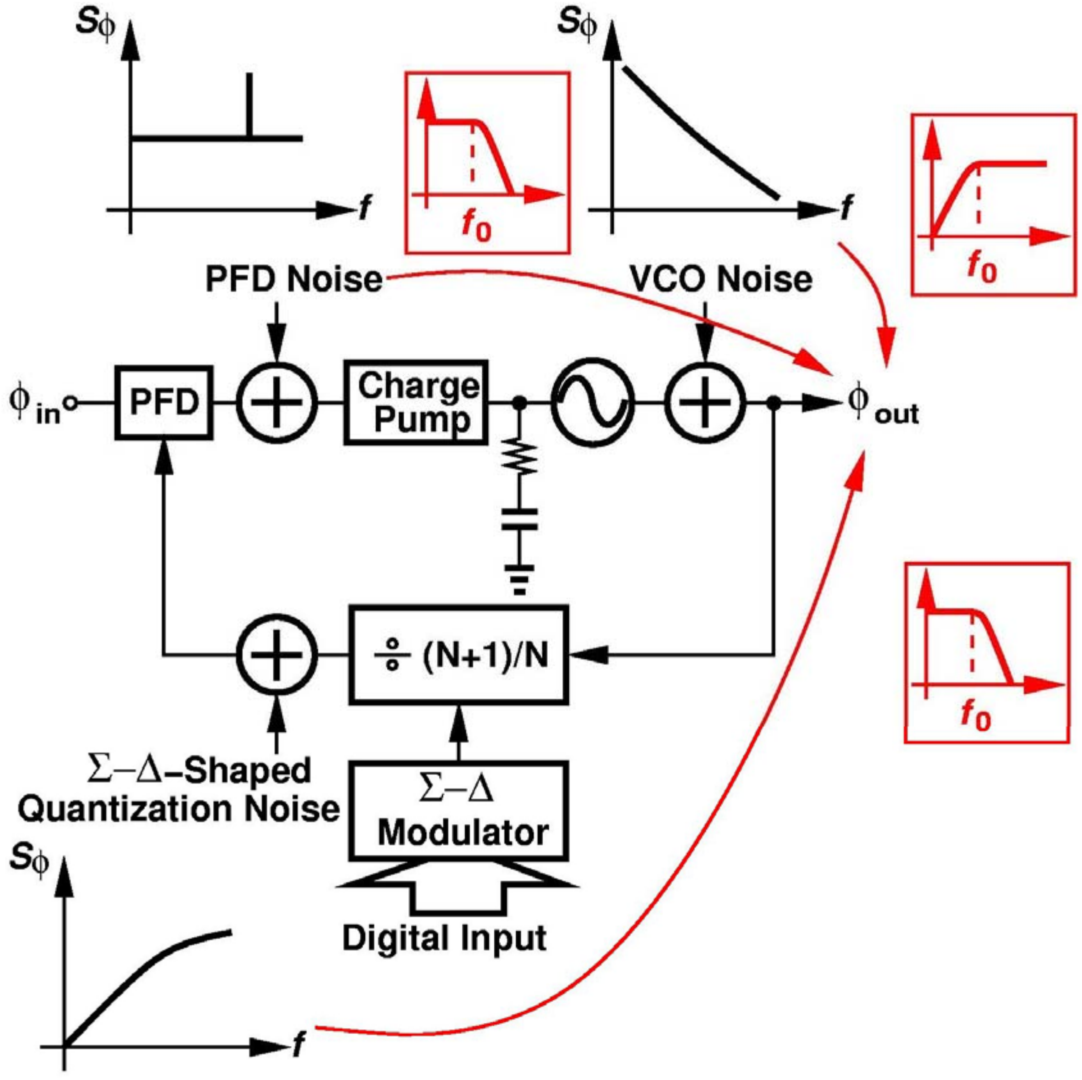
$$x[k] = 0.5 + 0.25\sin\left(\frac{2\pi}{100}k\right)$$





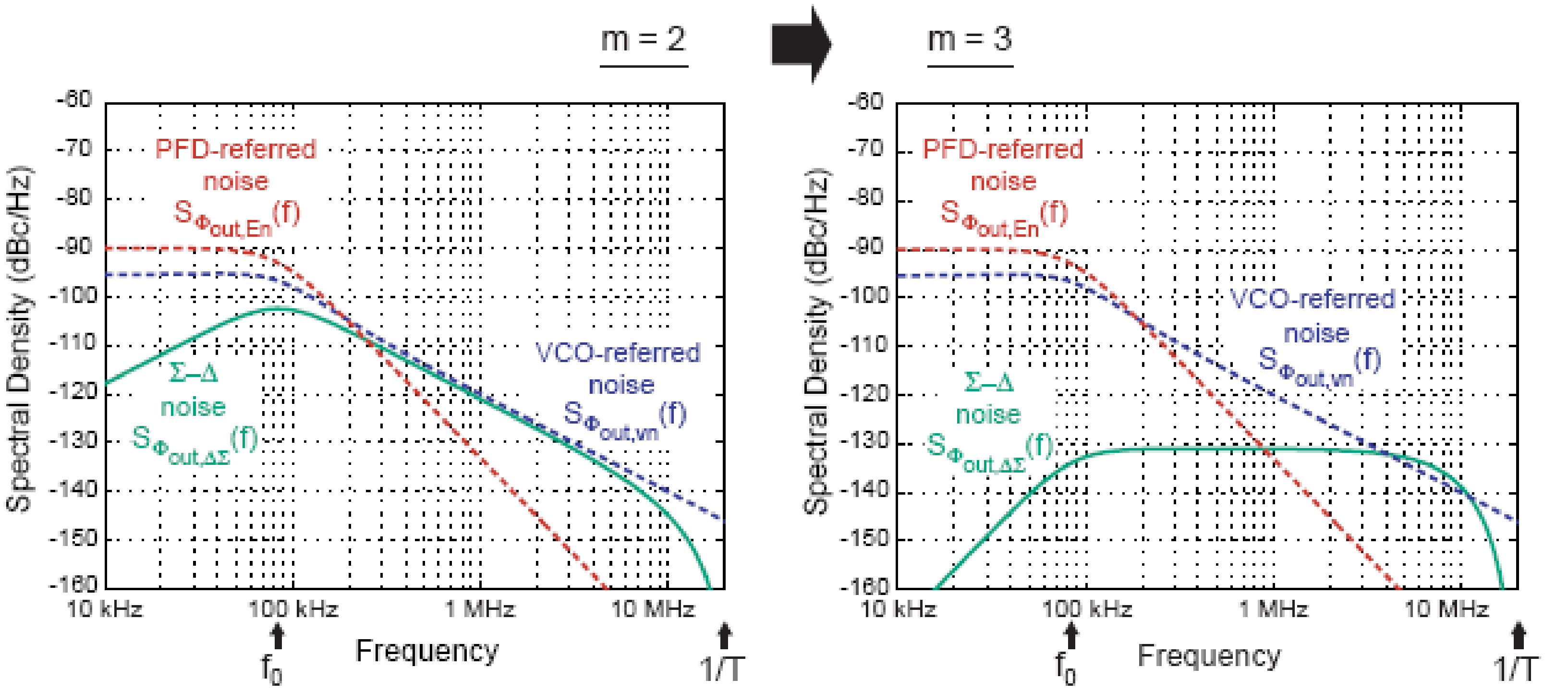
[Courtesy, M. Perrott]

Noise Analysis on Σ–Δ Frequency Synthesizers



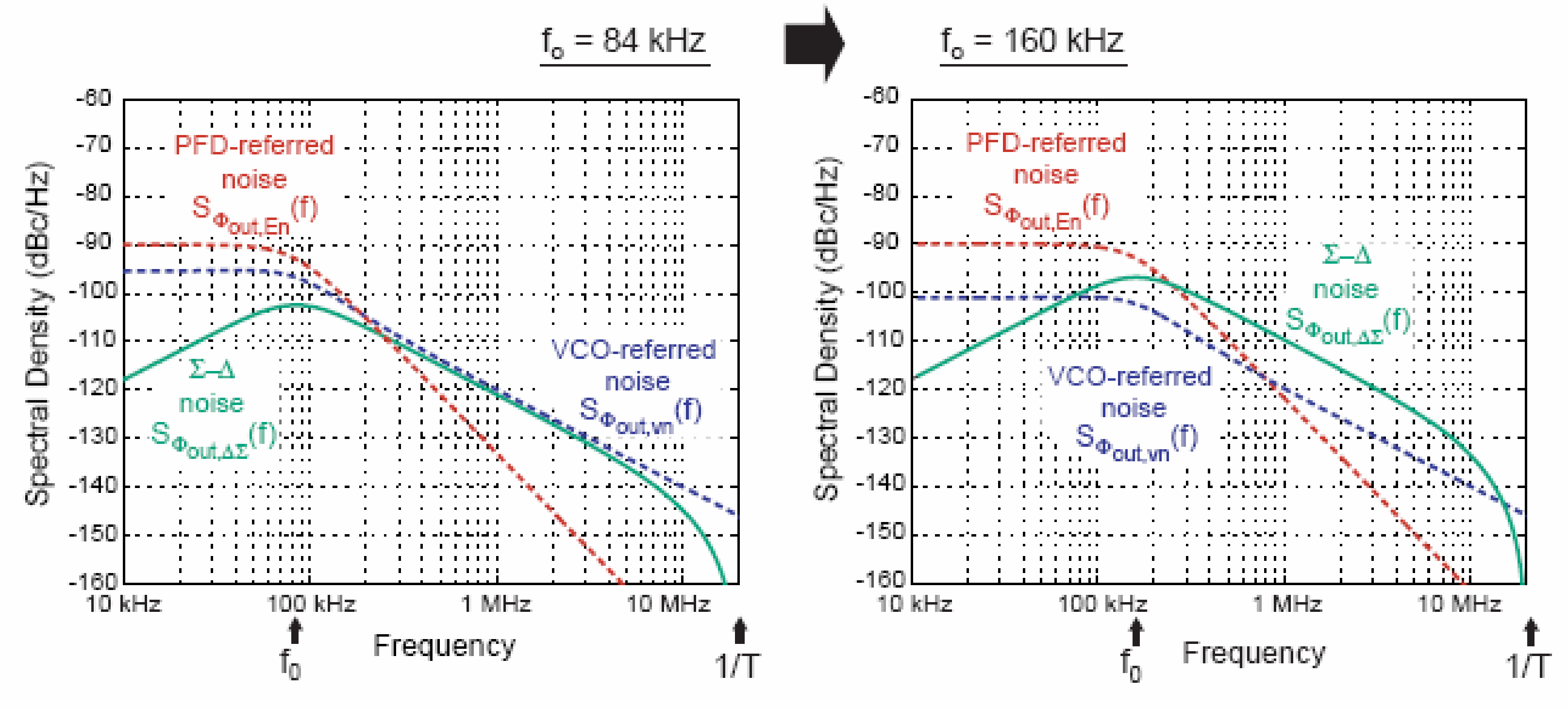
- Total noise is the combination of the three sources.

Well-Designed Σ–Δ Synthesizers



- Loop bandwidth low enough so that PFD and VCO noise dominate.
- Higher order Σ-Δ modulator shapes the quantization further but PFD and VCO noise unaffected.

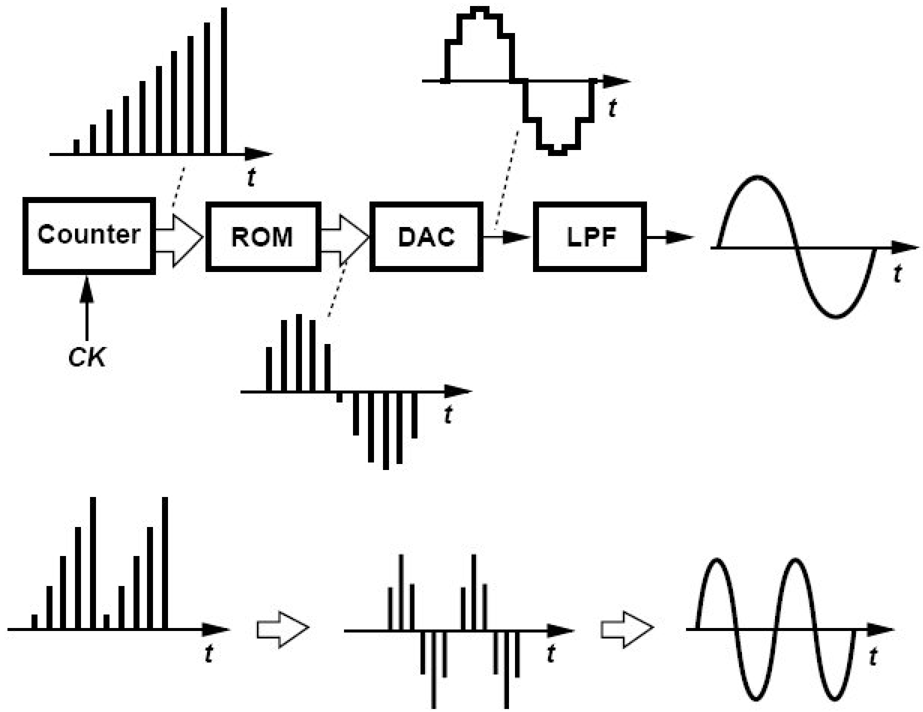
Impact of Loop Bandwidth



- Increase loop bandwidth => more PFD noise, more Σ-Δ noise, less VCO noise.
- The rule of thumb is to take the advantage of Σ-Δ modulator without degrading other performance.

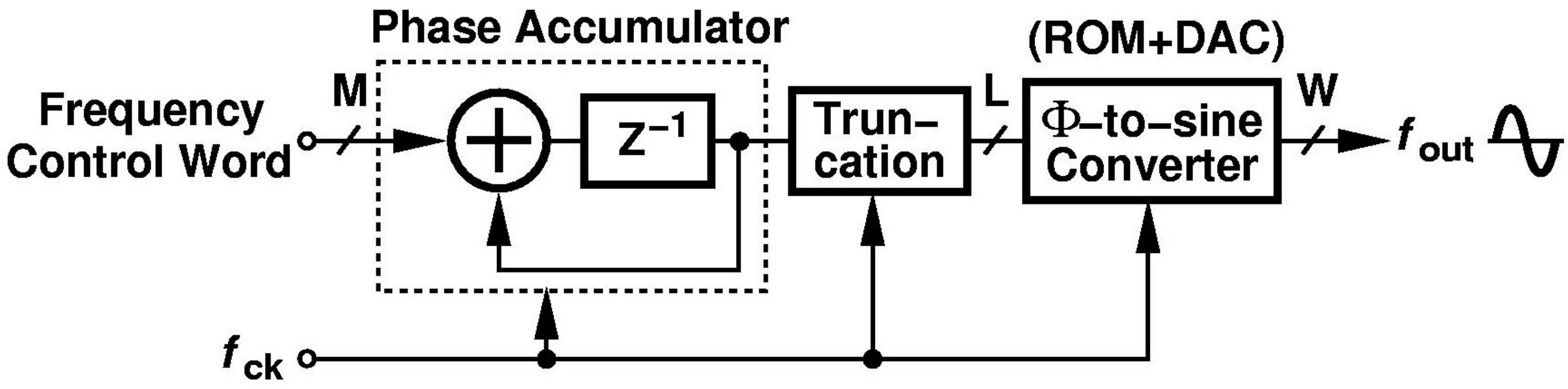
Direct Digital Frequency Synthesizers

- Can we synthesize a clock directly from database?



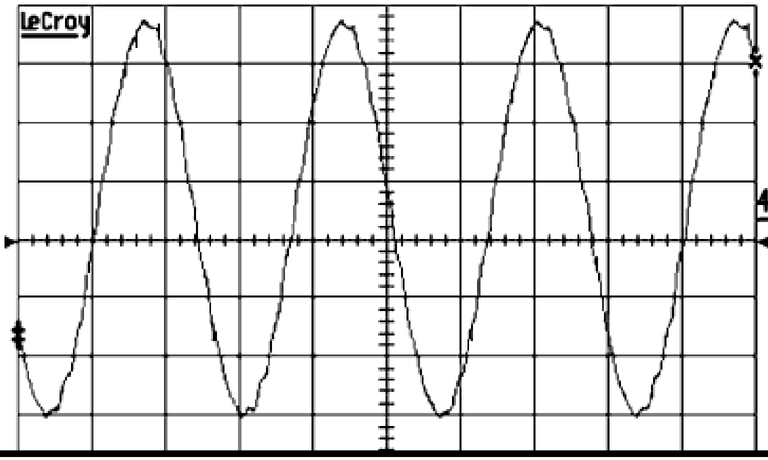
- **Advantages:**
  - Instant switching (*f* and ϕ)
  - Ultra low phase noise (≈ Xtal)
  - Direct modulation
- **Drawbacks:**
  - Speed
  - Waveform distortion

General Realization of DDFS

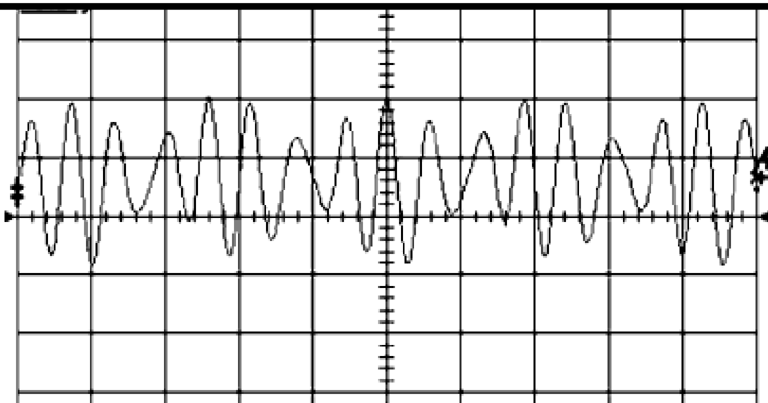


- Truncation and amplitude quantization cause spurs.
- ROM size (1/4 waveform).
- DAC resolution/speed.
- Unwanted modulation when f_{out} becomes comparable with f_{ck}.

General Issues of DDFS

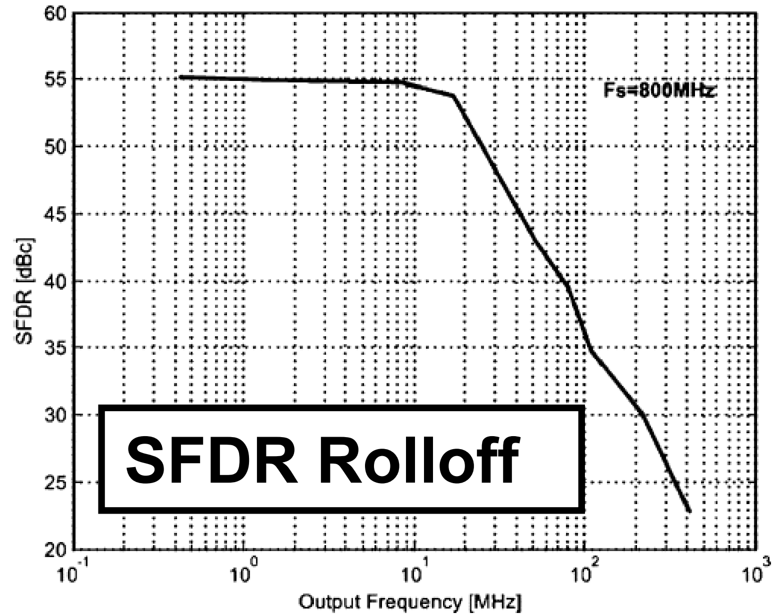


f_{ck} = 800MHz, f_{out} = 18MHz



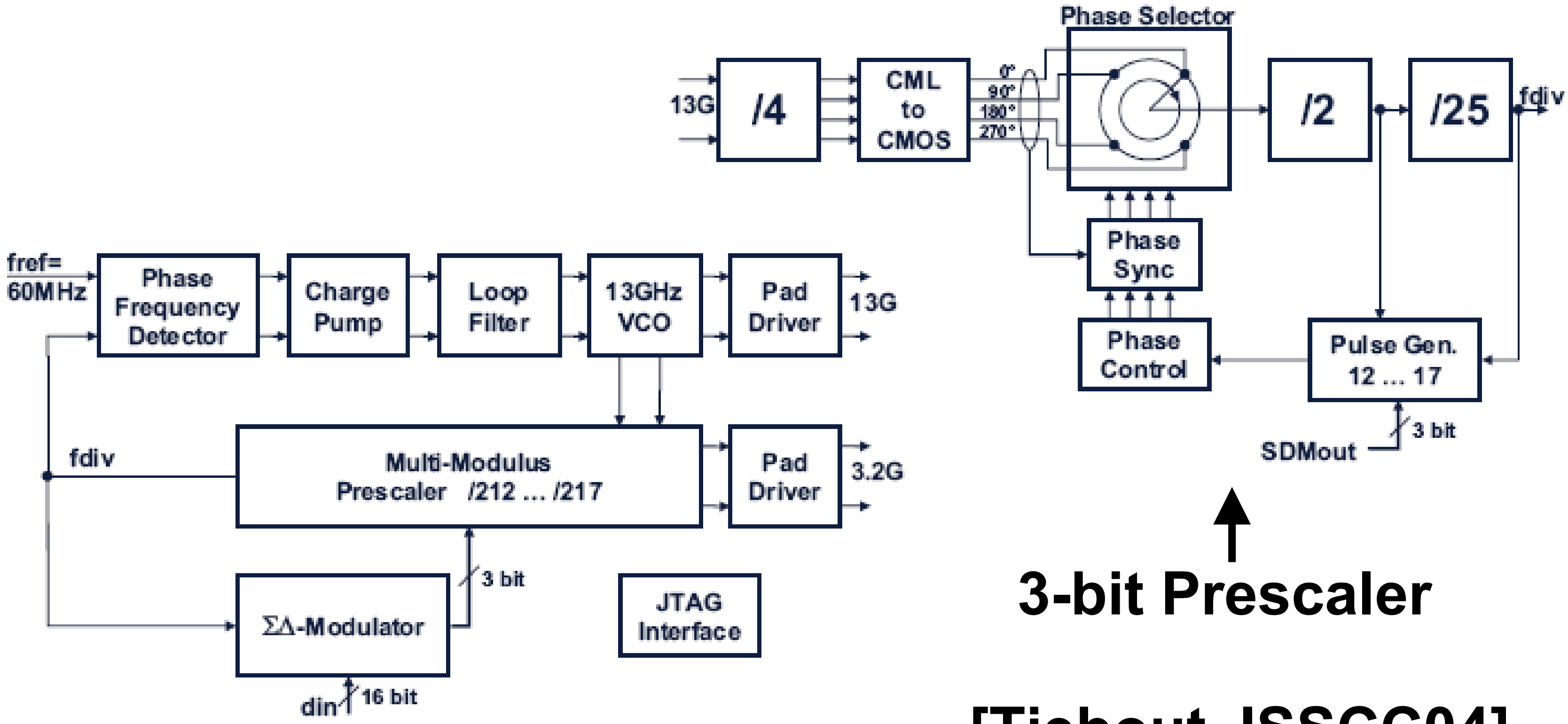
f_{ck} = 800MHz, f_{out} = 328MHz

Highly distorted



[Yang et al, JSSC04]

Case Study



3-bit Prescaler

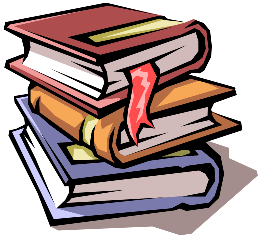
[Tiebout, ISSCC04]

- **13GHz Fractional-N PLL.**
- **Second order modulator.**

Clock and Data Recovery

Professor Jri Lee

台大電子所　李致毅教授



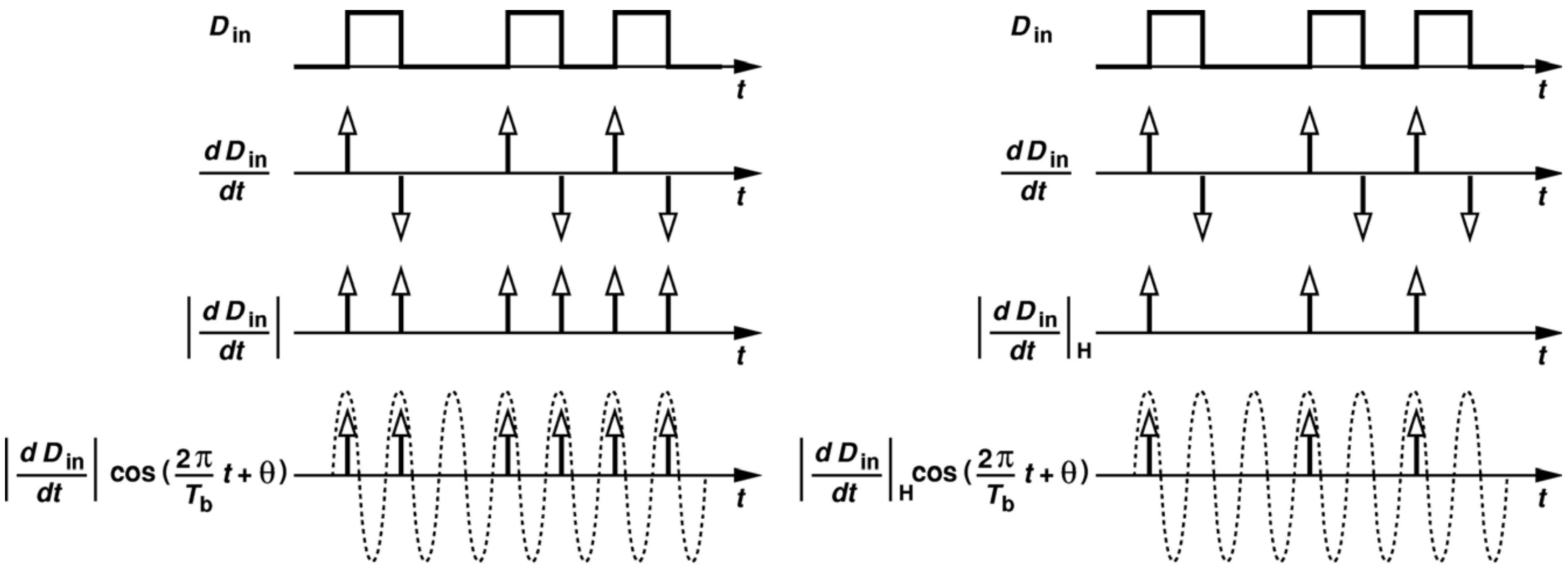
Electrical Engineering Department
National Taiwan University

Outline

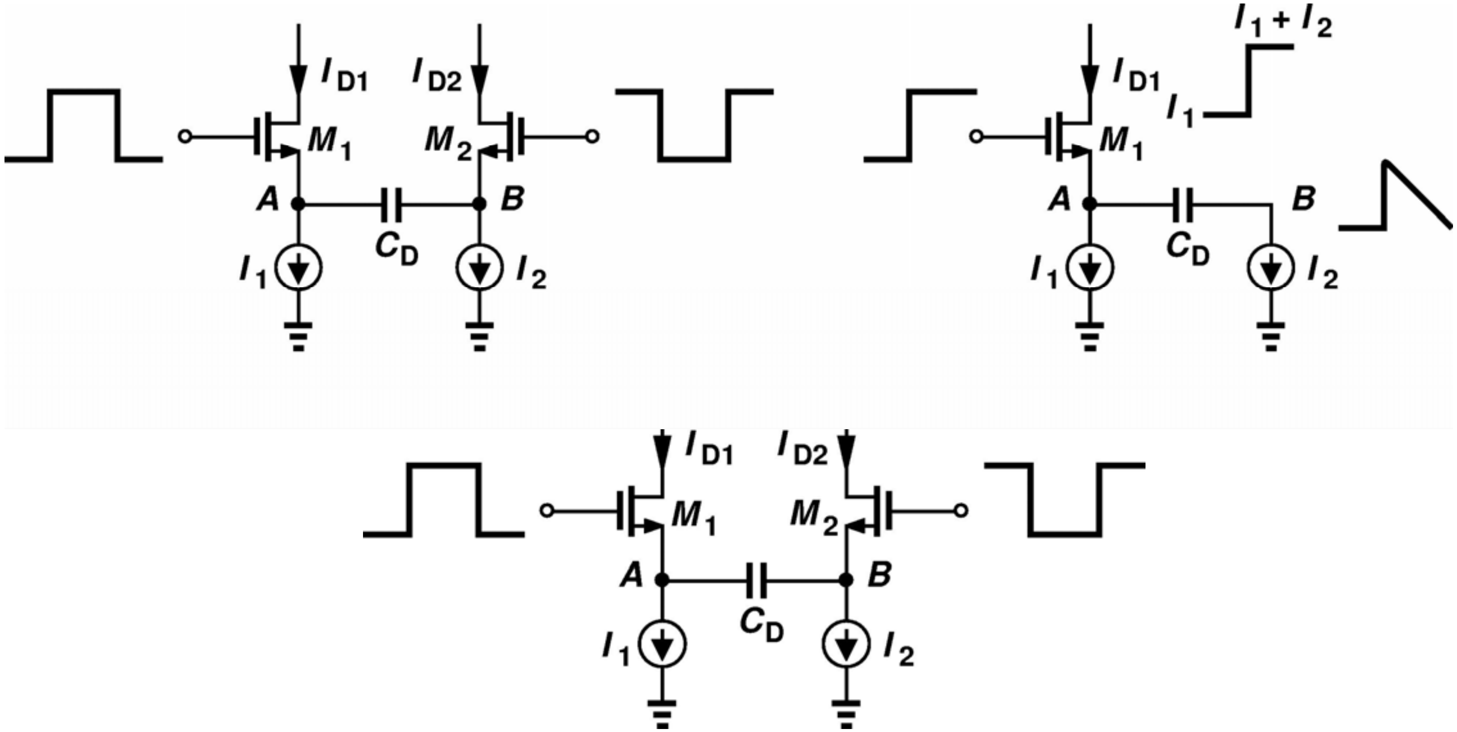
- General Considerations
- Linear Phase Detector
- Binary Phase Detector
- CDR Architecture

Edge Detection

- Extracting clock from NRZ data is not trivial at all, since its spectrum contains no power at the frequency of data rate.
- A circuit detecting the data transition is essential for clock recovery.

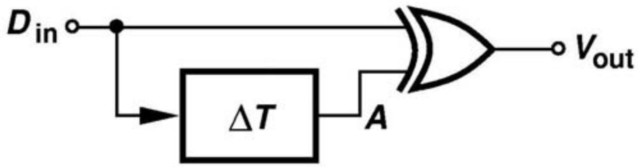


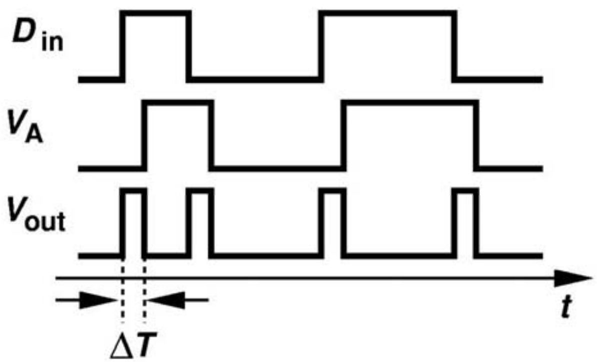
CMOS Realization of Edge Detectors

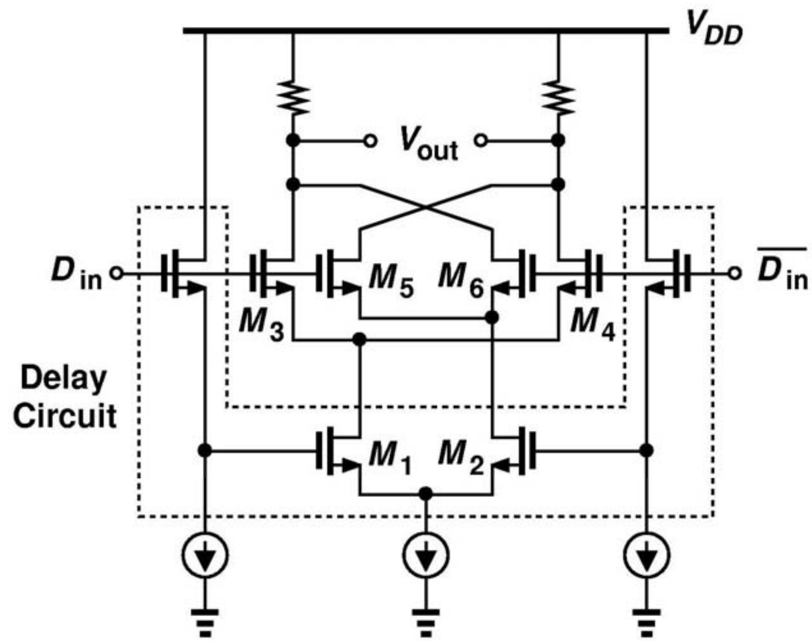


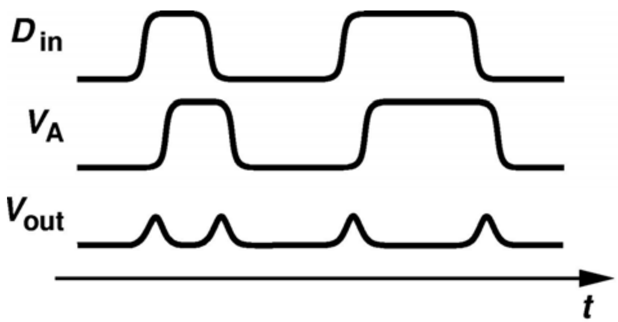
- Gilbert cell with capacitive degeneration may achieve differentiation and rectification at high speed.

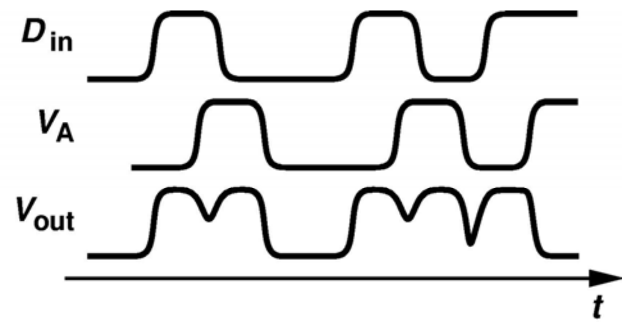
Alternative Solution for Edge Detection







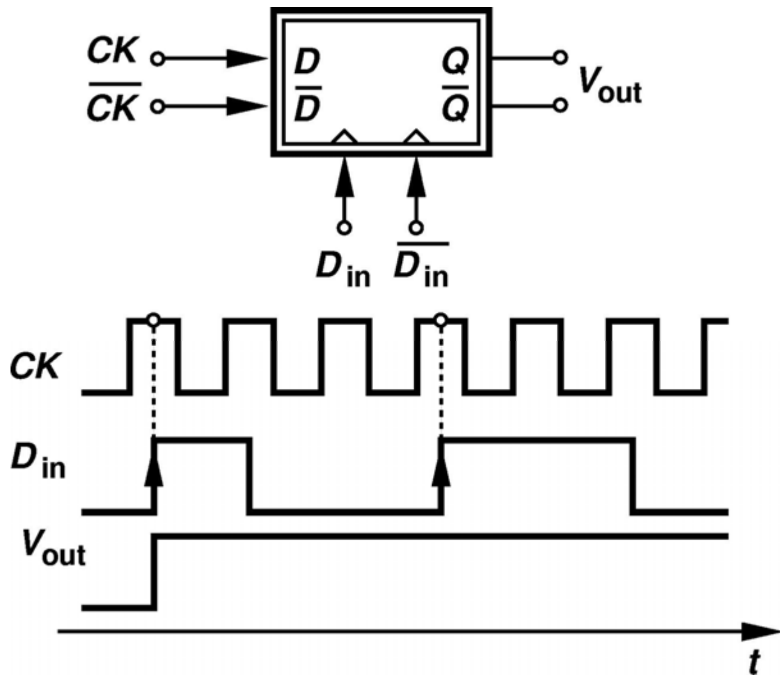


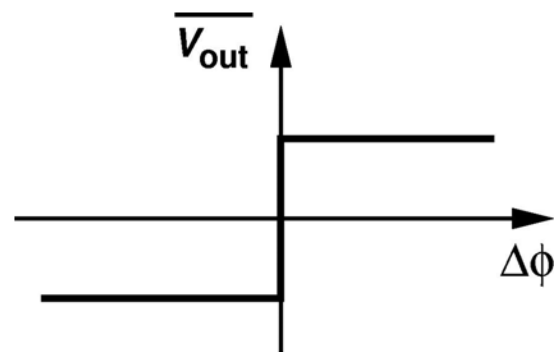


- Proper delay must be set to obtain clear pulses.
- PVT variation matters.

Phase Detection

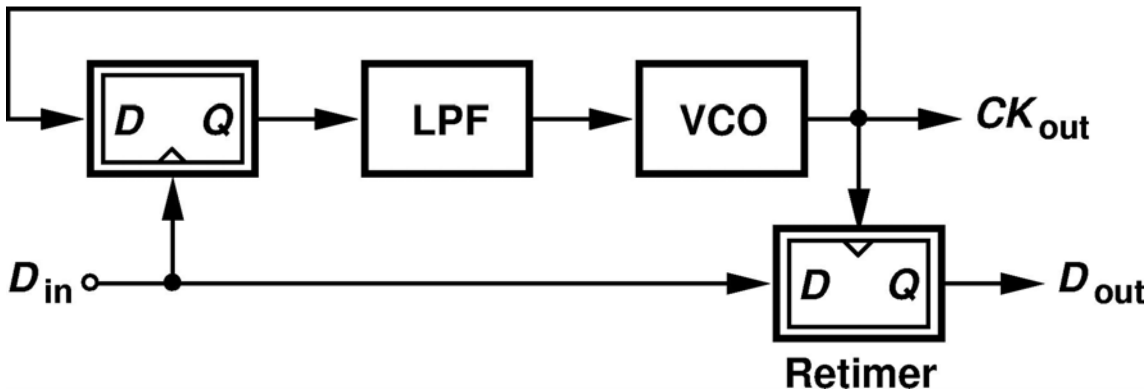
- A more efficient way is to detect the data transition and determine whether it is early or late with respect to its corresponding clock phase.





- Finite acquisition range (Why?)
- Binary characteristic

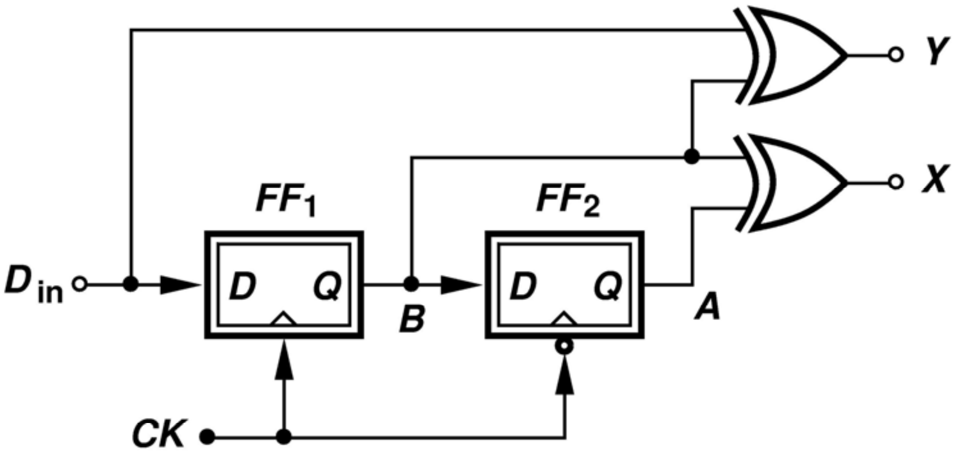
Simple CDR with Single-FF Phase Detector

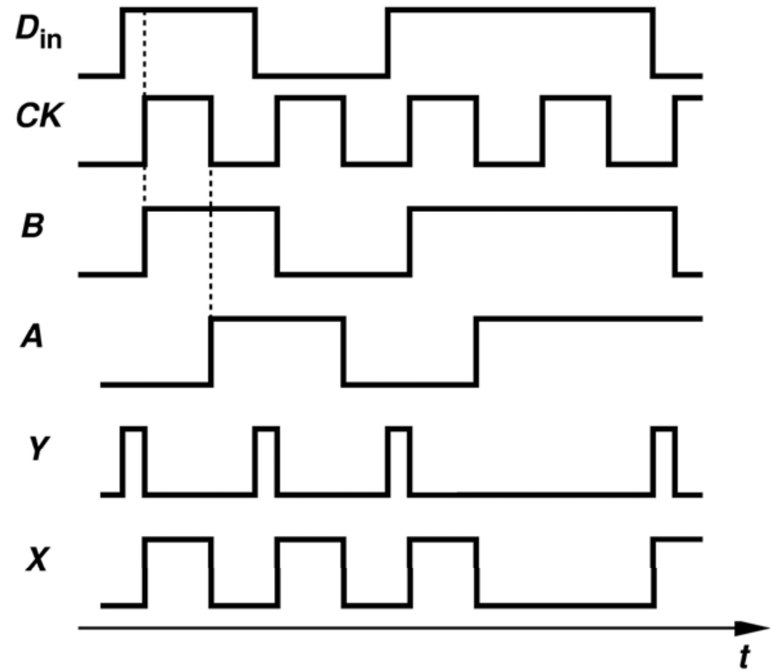


❒ **Drawbacks:**

- **Continue to increase or decrease the VCO control voltage even when no data edge is present $\Rightarrow$ large jitter.**
- **Large skews may cause improper sampling.**
- **Finite capture range (lack of frequency acquisition loop).**

Hogge Phase Detector

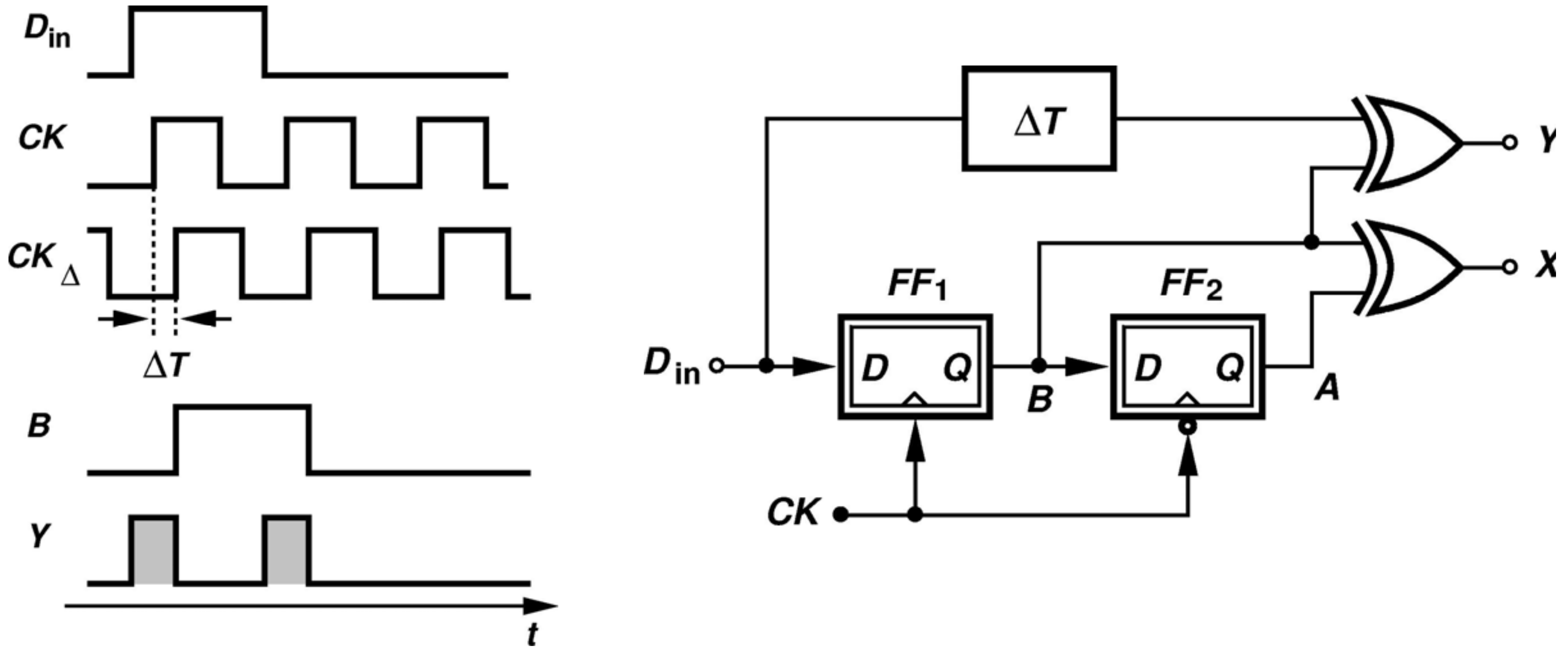




[Hogge, ’85]

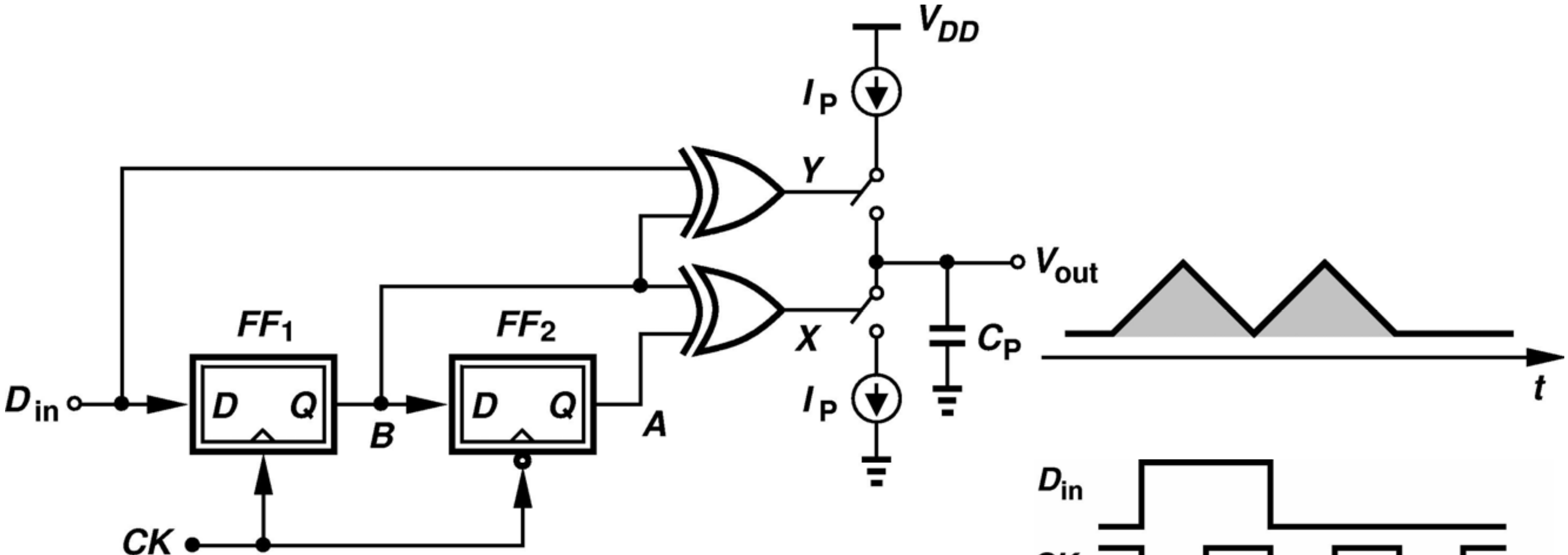
- Linear operation.
- Complete pulses must be generated within approximately 1/4 of a bit period.
- Suitable for low to moderate frequency.

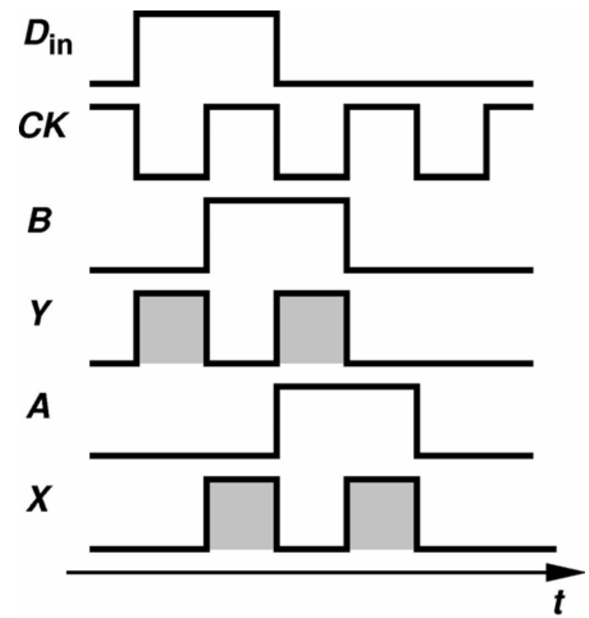
Non-idealities of Hogge Phase Detector



- FF delay requires compensation.
- Δ*T* may not track the FF delay well across a wide range of temperature and supply variations.
- Generating a delay of several tens of picoseconds is not easy in terms of power and/or area.

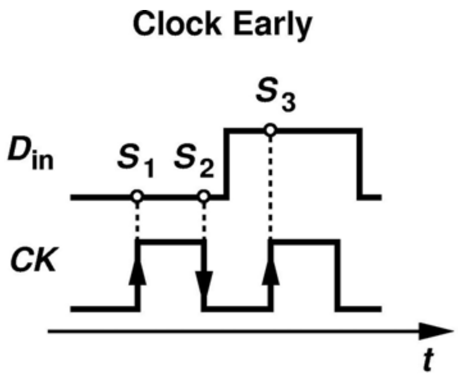
Tri-Wave Issue

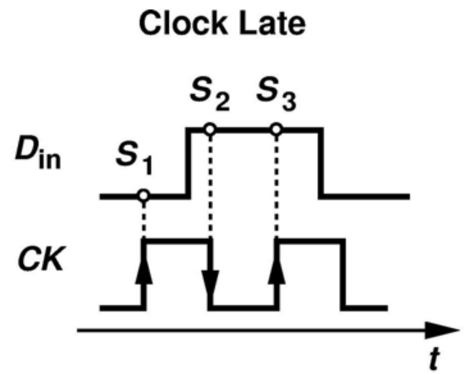


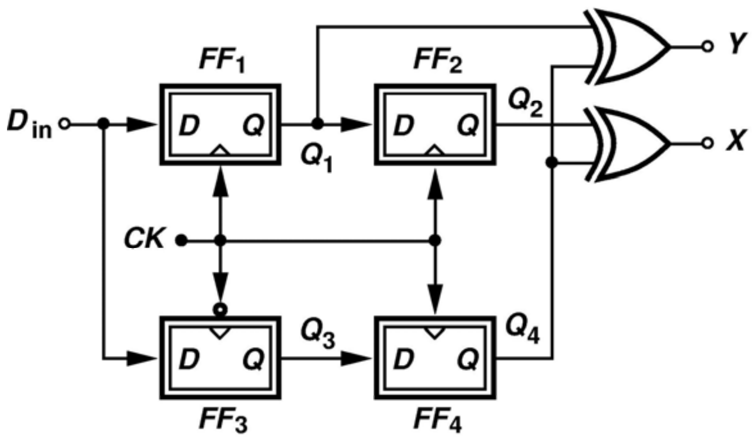


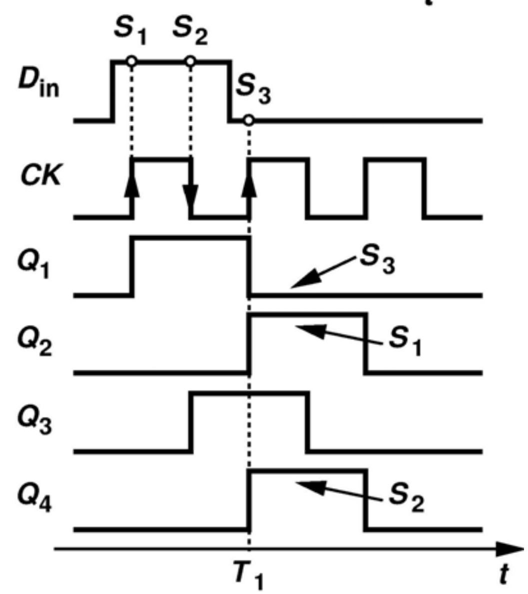
- UP and DOWN pulses are not aligned in time, creating tri-waves on the VCO control lines.

Alexander (Bang-Bang) Phase Detector





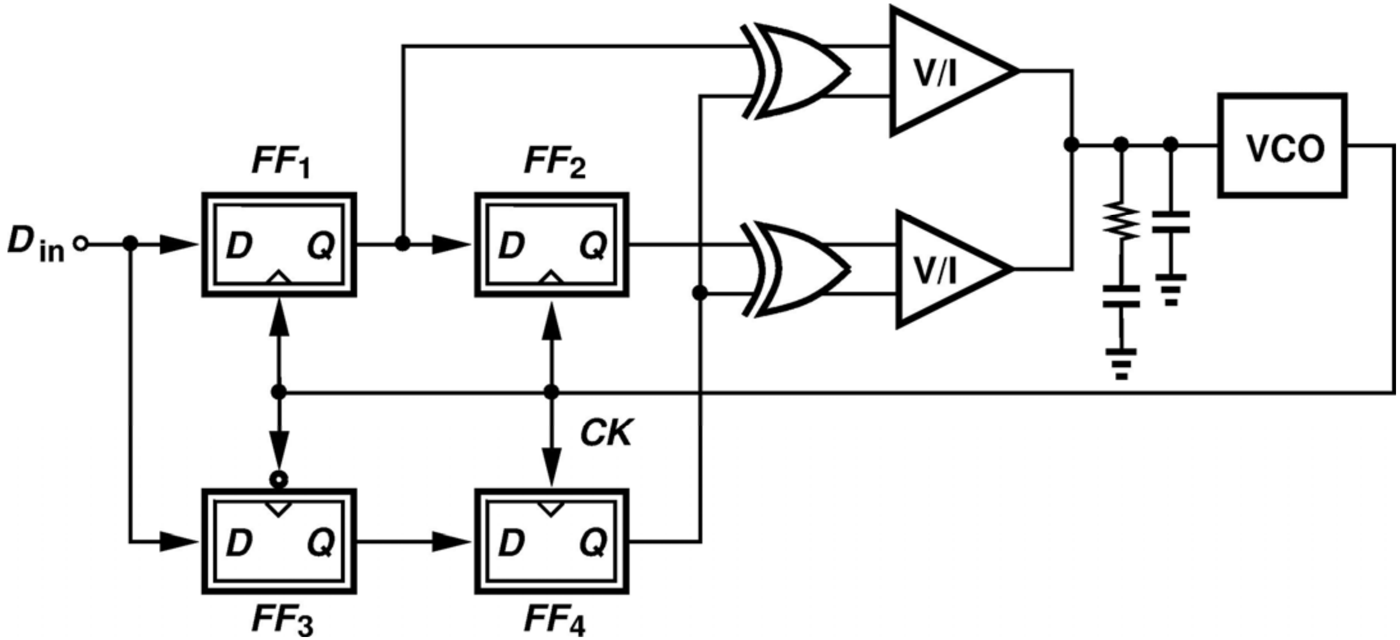




[Alexander, '76]

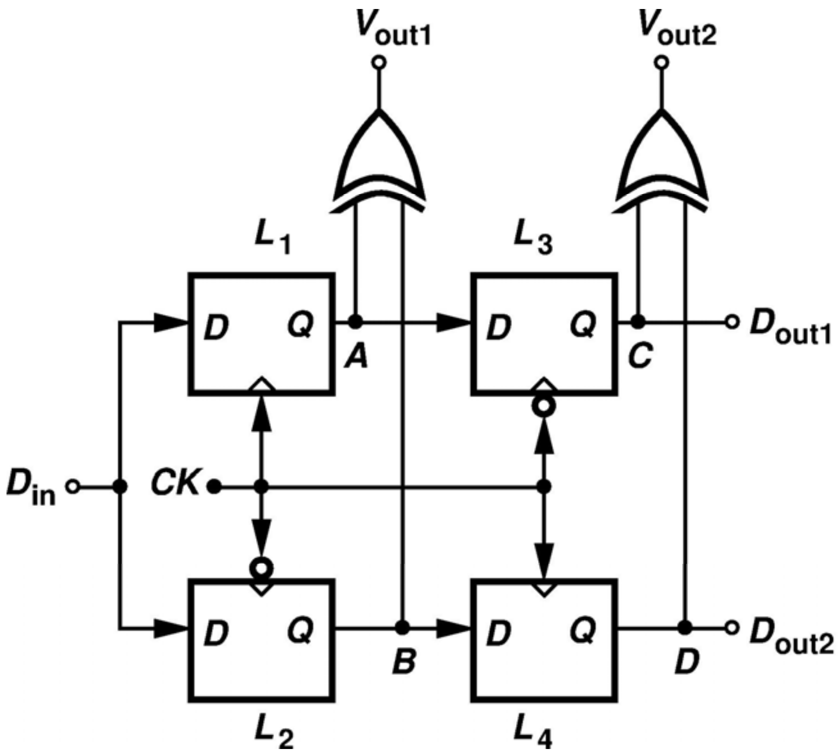
- Binary operation simplifies the phase comparison and increases the speed.
- Abruptly toggling between two states rather than gently waggling around zero.

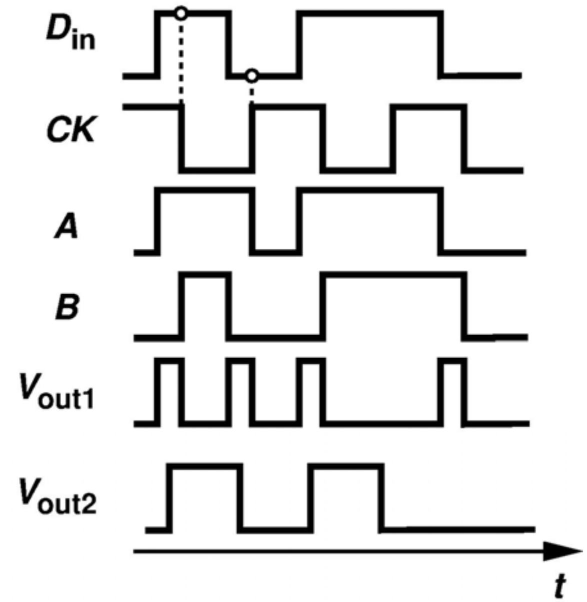
Complete CDR using Alexander PD



- Both Hogge and Alexander PDs provide automatic data retiming and tri-state output (i.e., no net current during long runs).
- Both Hogge and Alexander PDs have only limited capture range and require frequency acquisition loop.

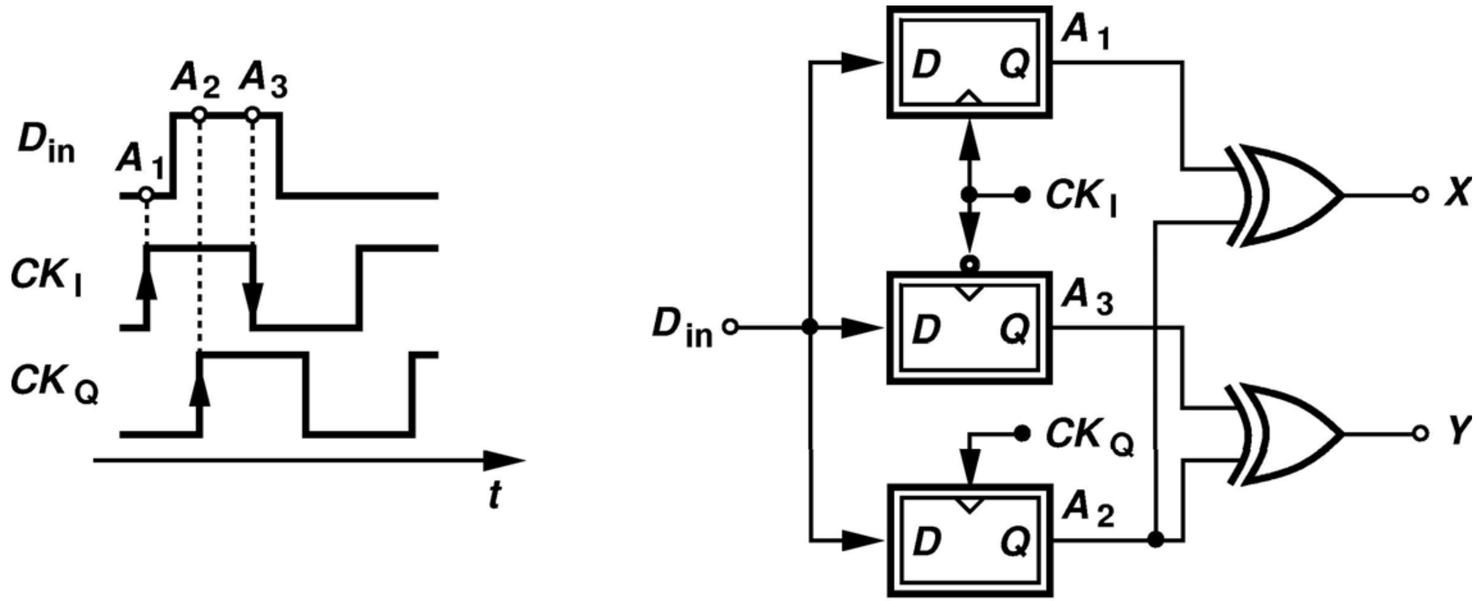
Half-Rate Hogge Phase Detector





- C ⊕ D serves as a reference.
- Clock duty cycle plays crytical roles (must be 50%).

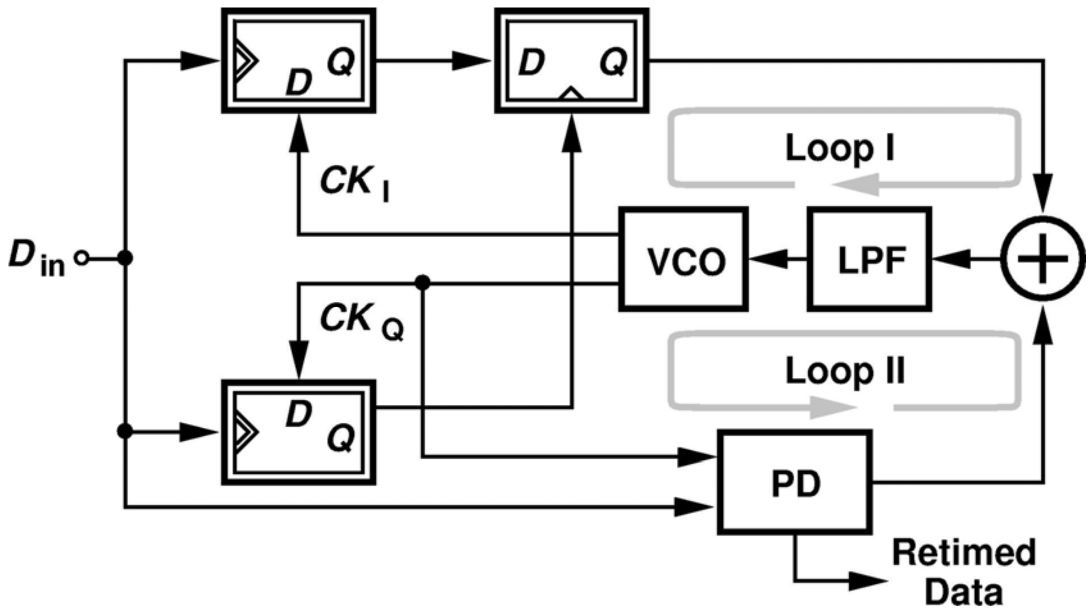
Half Rate Alexander Phase Detector



- Clock with quadrature phases is a must.
- Many other ways to implement sub-rate CDRs (how about quarter rate?)

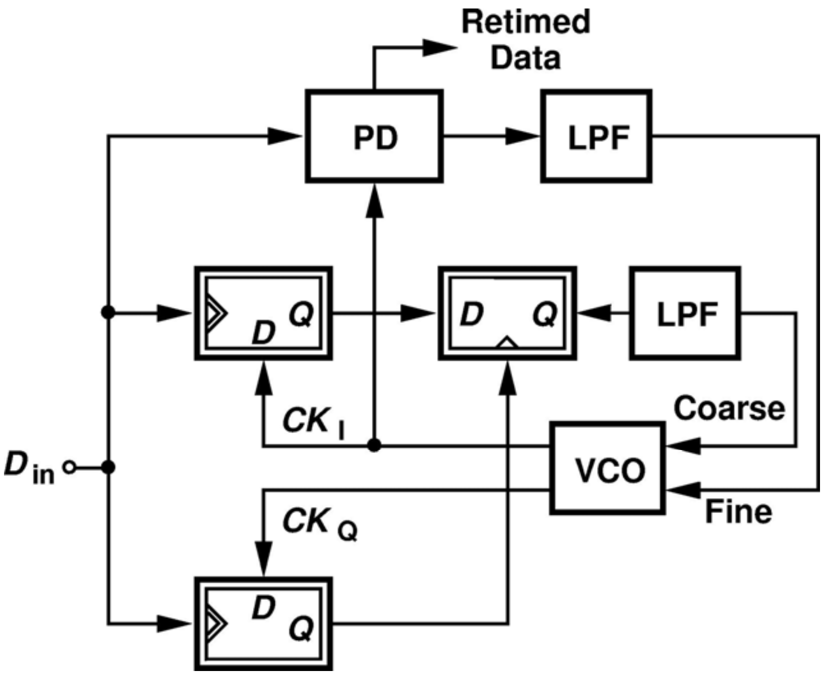
CDR Architecture

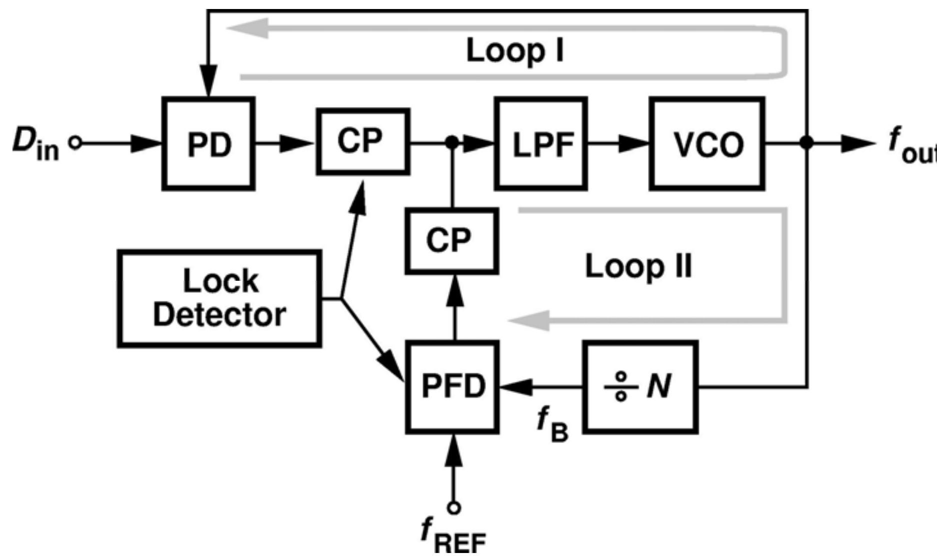
- For most CDRs, the acquisition range is roughly equal to the loop bandwidth, which is about 1/1000 of the data rate.
- Such a small range mandates the use of additional frequency acquisition loop.



- One set of system parameters must satisfy two loops.

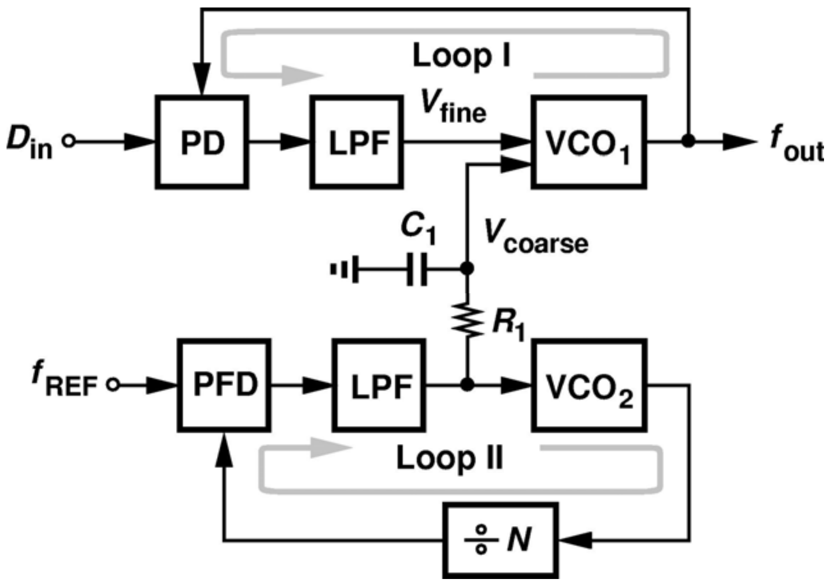
Alternative CDR Architectures

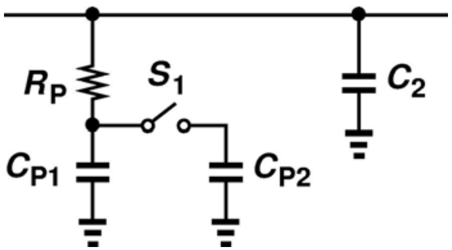




- FD loop pushes the oscillation frequency to roughly-right position.
- PD loop then takes over to lock the phase.
- Lock detector is required to shut down the FD upon lock.

Alternative CDR Architectures

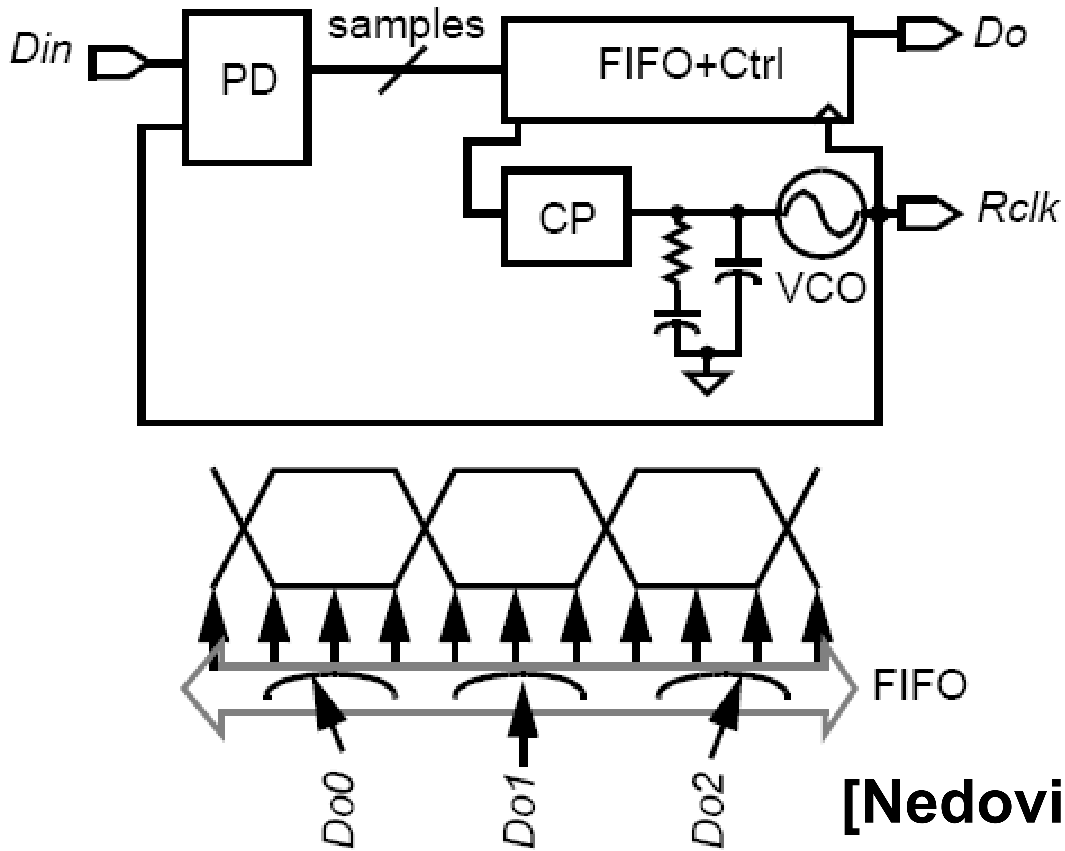




Adjustable Parameters

- Proper logic and timing control is required for a smooth switching.
- But after all, it is the PD loop that determines the performance in lock.

Case Study – 40Gb/s Over-Sampling CDR



[Nedovic, ISSCC07]

- 3x over sampling.
- Quarter-rate VCO.